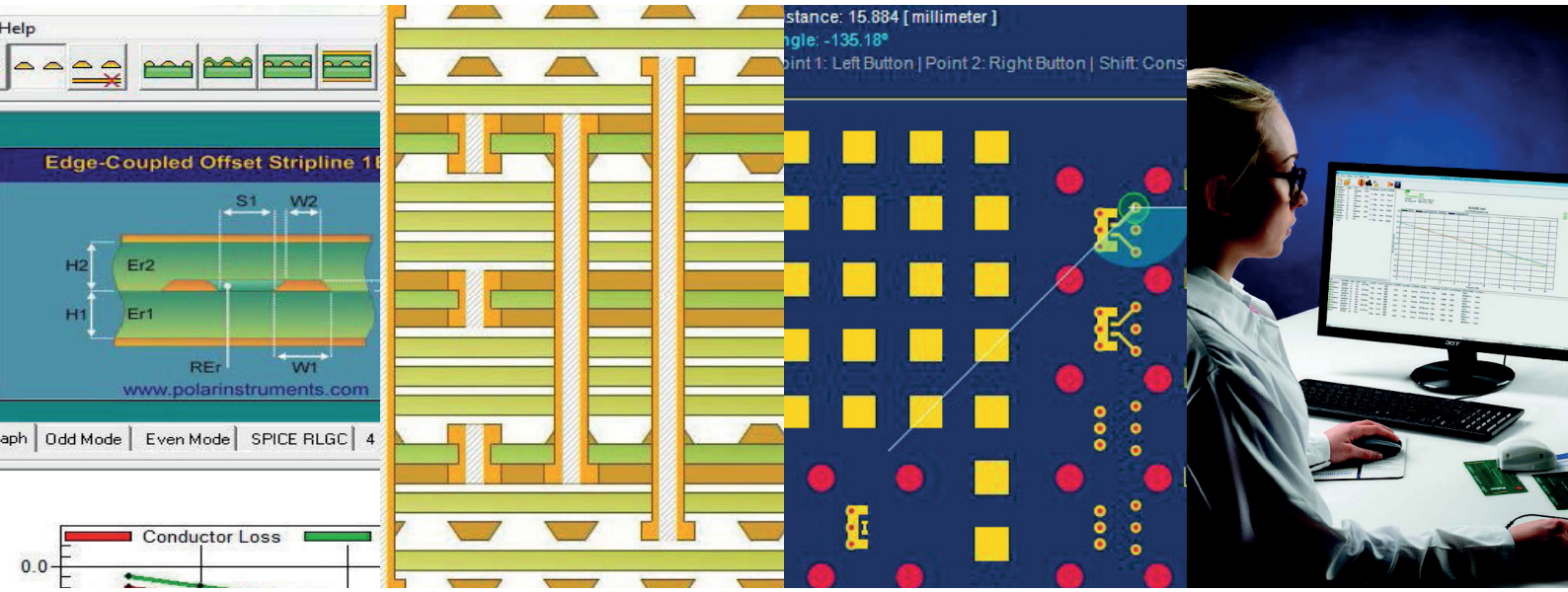
Controlled Impedance PCBs



An Introduction to the Design and Manufacture of Controlled Impedance PCBs with Insights into Insertion loss.

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Introduction

We produced the first edition of this booklet several years ago in response to many requests for a basic introduction to the manufacture of controlled impedance printed circuit boards (PCBs). In this third issue we have added extra material to some sections and introduced a number of new topics to reflect the changes that have occurred in the industry over the last few years, including measuring traces with thin copper and small geometries, plus a new section on the growing topic of insertion loss. We have tried to explain the most important concepts and address the most frequently asked questions with the minimum of technical jargon.

You can download this document as a pdf file from polarinstruments.com or alternatively, ask your local distributor or Polar Instruments if you require further copies. If you would like more detailed information please look at both the application notes on the Polar website and the video content on the Polar Youtube channel.
www.youtube.com/polarinstruments

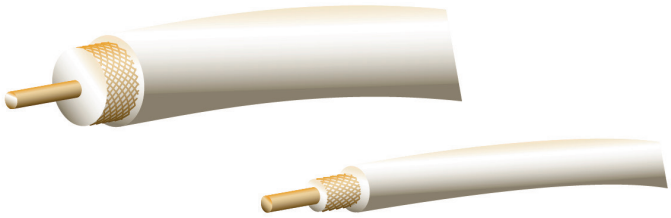
We hope that you find it useful and welcome any comments you may have, e.g. areas where you would like more detail, suggestions for new topics.

Page

What is controlled impedance?

The cable that connects the antenna to the television is a common example of a controlled impedance that most of us are familiar with.

Note: “Impedance” is a widely used term in electronics with different meanings often based on the context of the discussion. In the context of PCB transmission lines. Controlled impedance is actually referring to controlled *characteristic* impedance. i.e. It is the characteristic impedance of the PCB transmission lines that the designer and fabricator are setting out to control.



This cable may be one of two types, a coaxial cable consisting of a round inner conductor separated from the outer cylindrical conductor (the shield) by an insulator. The dimensions of the conductors and insulator and the electrical characteristics of the insulator are carefully controlled in order to determine the shape, strength and interaction of the electrical fields which in turn determine the electrical impedance of the cable.

Instead of a coaxial cable, an antenna may be connected to the TV by means of a cable formed of two round wires spaced by a flat strip of plastic. As with the coaxial cable, the dimensions and materials of this wire are carefully controlled so as to give it the correct characteristic impedance.

These two cables are examples of different configurations of a controlled impedance but there are many others. In the same way, you will learn that there are many different trace configurations that are used in the PCB industry to achieve a controlled impedance. Controlled impedance PCBs emulate controlled impedance cables, where the coax shield may be represented by a plane, the insulator represented by the laminate and the conductor is the trace. Just as for the cables, the impedance is determined by the dimensions and materials, and these parameters must be very carefully predicted in design and then controlled in the manufacturing process to ensure that specifications are met.

Impedance is measured in Ohms (symbol Ω) but is not to be confused with resistance, also measured in Ohms (also with symbol Ω).Resistance is a DC characteristic, whilst impedance is an AC characteristic which becomes important as the signal frequency increases, typically becoming critical for PCB traces at signal components of two or three hundred MHz and above.

Why do we need controlled impedances?

The function of a wire or trace is to transfer signal power from one device to another. Theory shows that maximum signal power is transferred when impedances are matched. A TV antenna has a “natural” characteristic impedance. At RF frequencies of between hundreds of MHz (megahertz) and GHz (gigahertz) the transfer of maximum signal power from the antenna to the cable requires that the cable impedance match the antenna impedance. Also, the TV impedance must match the cable impedance. Hence, there is a matched system where the antenna to cable to TV impedances all closely match and the maximum amount of signal is transferred from the antenna to the cable and thence to the TV.

Where there is an impedance mismatch, maximum signal power transfer does not occur. Only a portion of the signal power is transferred from the sending device into the receiving device (coax, PCB trace, etc.) The remainder of the signal power is reflected back to the sending device.

Suppose a cable of incorrect impedance links the antenna to the TV. Thus, the TV antenna and the cable impedance do not match, and not all of the TV signal detected by the antenna will pass from the antenna into the cable. Some will be reflected back into the antenna and be re-radiated. Thus the TV will not receive the maximum signal available and the picture may pixelate or freeze momentarily.

Next, since the cable impedance does not match the TV impedance, not all of the signal conveyed by the cable will pass into the TV. Some will be reflected back into the cable, resulting in a further loss of available signal to the TV. But this is only the start of the problem. The reflected signal will travel back along the cable to the antenna, where it will encounter the impedance mismatch again and another partial reflection of the signal will occur. This reflected signal will reduce the effective data rate that the TV receives and the result will be a reduction in resolution or worse the picture may tear up and freeze. Thus the picture (data) has been corrupted by signal reflections caused by impedance mismatches.

Impedances Matched

Impedances Mismatched

The consequences are slight in this example – a degraded TV picture. But suppose that the signal had been carrying bank data in the form of binary ones and zeros. What could have happened if a zero had bounced back and forth in the cable and had corrupted your personal account information?

“Sorry, your account is overdrawn”

Types of systems that use controlled impedance PCBs

Although we have focused on wire interconnections, exactly the same considerations apply to signal transfer through traces on a PCB. When board traces carry signals containing high frequencies care must be taken to design traces that match the impedance of the driver and receiver devices. The longer the trace, or the greater the frequencies involved, then the greater the need to control the trace impedance. The PCB manufacturer controls the impedance by varying the dimensions and spacing of the particular trace or laminate.

Any impedance mismatch can be extremely difficult to analyse once a PCB is loaded with components. Components have a range of tolerances, so that one batch of components may tolerate an impedance mismatch while another batch might not. Moreover, a component's characteristics may change with temperature, so that the problems may come and go. Thus, if changing a component appears to cure a problem, the components may become the suspects instead of the trace. Component selection becomes the solution, and build costs are driven up, while all the time the real fault – trace impedance mismatch – goes undetected!

For these reasons a PCB designer will specify trace impedance and tolerance and should work with the PCB manufacturer to ensure that the PCB meets the specifications.

Controlled impedances on PCB traces

Over time, more and more PCB designs need to take into account impedance control

* telecommunications
* video signal processing
* high speed digital processing
* real time graphic processing
* process control

Most homes today have numerous applications of these technologies, for example

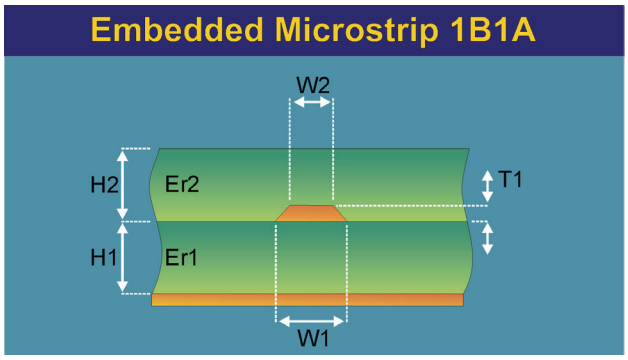
* Routers, cordless phones, satellite TV, internet TV
* Video games, phones
* Low cost personal computers, laser printers
* Home automation
* Auto engine control modules
* Infotainment modules
* Driver assistance, GPS navigation

Industry and commerce are awash with these same technologies, and the lists are continually expanding. Since this guide was first published virtually all PCBs include at least some controlled impedance traces. Controlled impedance has become the norm and insertion loss is growing as data rates increase well into the multi gigabit/s range.

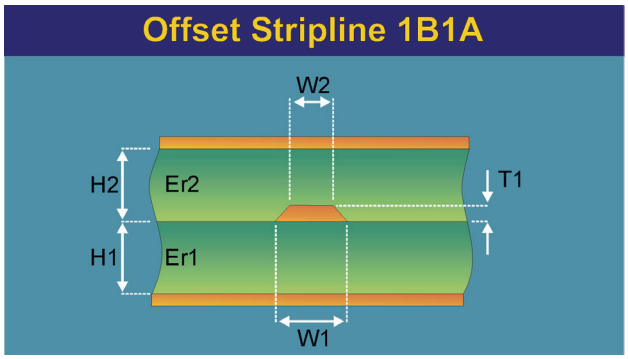
Examples of PCB controlled impedances

These diagrams are examples of some of the many different configurations that PCB designers can use. When you are looking at the stack up of a multilayer PCB, remember that controlled impedances are shielded by planes and for this reason, you only need consider the laminate thicknesses between the planes on planes above and below the trace when it is inside the PCB.

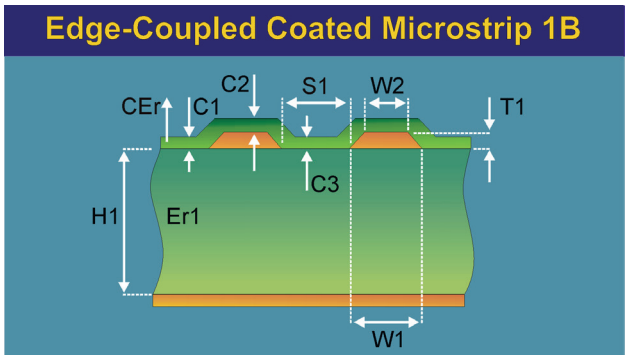
Embedded Microstrip contains a trace sandwiched within the PCB with a plane on one side and laminate and then air on the other.



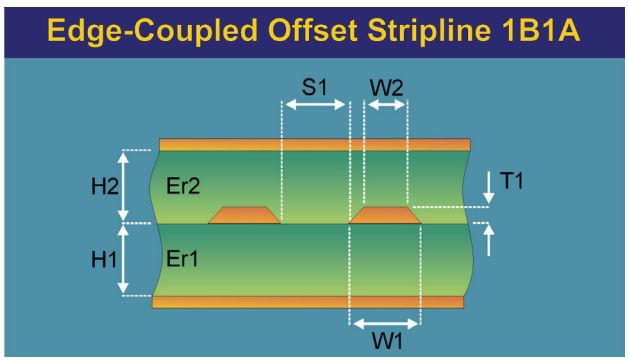
Offset Stripline contains a trace sandwiched within the PCB with a plane on both sides of the laminate.



Edge coupled coated microstrip is a differentialconfiguration where there are two controlled impedance traces on the surface, coated by resist and a plane on the other side of the laminate.

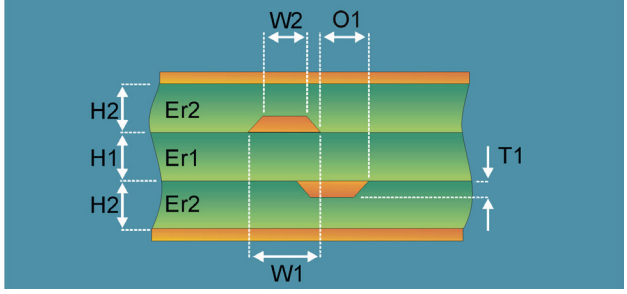


Edge coupled offset Stripline is a differential configuration with two controlled impedance traces sandwiched between two planes. The traces are shown offset, however they could be midway between the planes.



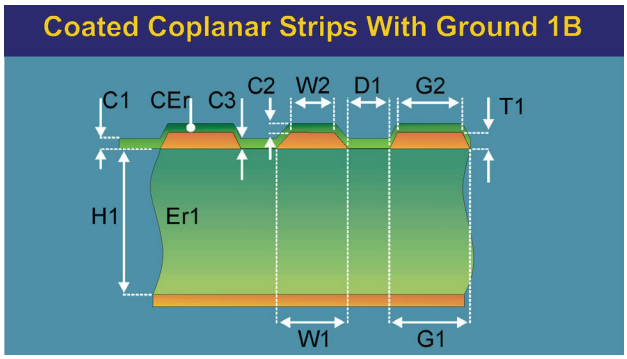
This differential configuration has two traces that are separated by laminate and sandwiched between two planes. Although the diagram shows the traces offset, the manufacturing objective is to have the traces with no offset, i.e. one should be directly above the other. Typically, this configuration is difficult to fabricate.

Broadside-Coupled Stripline 2S



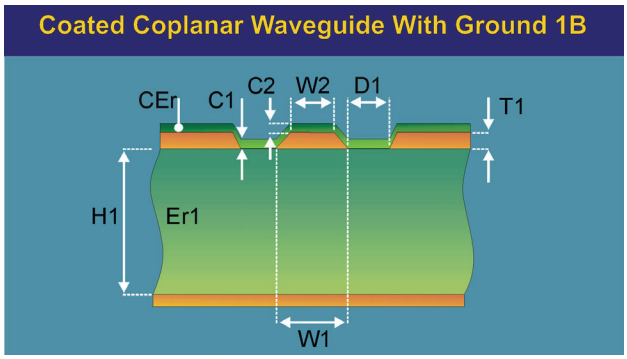
In this Coated Coplanar Strips configuration, there is a single controlled impedance trace with two ground traces of a specified width (G1/G2) either side. All the traces are coated with resist.

Coated Coplanar Strips With Ground 1B



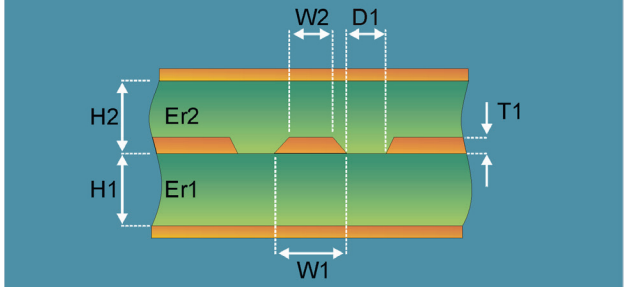
The Coplanar Waveguide has a single controlled impedance trace with planes either side (or very wide ground traces), a continuous plane on one side and laminate only on the other side.

Coated Coplanar Waveguide With Ground 1B



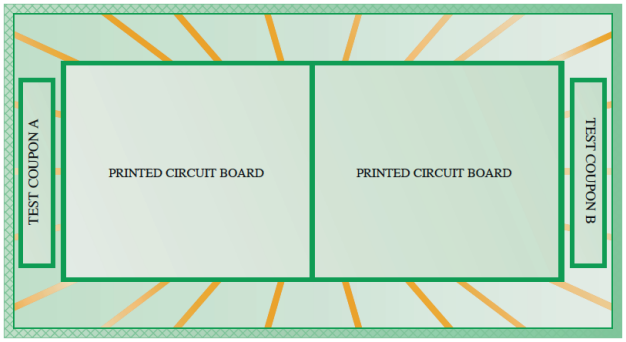
This Coplanar Waveguide is similar to the above configuration except that there are planes on both sides of the laminate as well as a plane on the same layer as the controlled impedance trace.

Offset Coplanar Waveguide 1B1A



As the operating speed of electronic circuits has increased, so has the need for PCBs to have controlled characteristic impedances and the majority of PCB manufacturers are producing them. As described earlier, if the value of characteristic impedance is incorrect, it can be very difficult to identify the problem once the PCB is assembled. Since the impedance depends on many parameters (trace width, trace thickness, laminate thickness, etc.) the majority of PCBs are currently 100% tested for controlled impedance. However the testing is not normally performed on the actual PCB but on a test coupon manufactured at the same time and on the same panel as the PCB. Sometimes the test coupon is integrated into the main PCB.

Sometimes your PCB customer is not aware that testing is best accomplished using test coupons and you, as the PCB manufacturer, will need to explain the benefits of coupons which include:



Typical Production Panel

All ground and power planes are connected together on test coupon only.

Same aperture codes are used on coupon as on board.

* It is rare for controlled impedance traces to be easily accessible for testing (including a closely situated ground connection).
* Planes are not interconnected on the main PCB and this may lead to inaccurate measurements.
* Accurate and consistent testing results require a straight single trace of 150mm (or longer), often the actual PCB trace is shorter than 150mm.
* The actual PCB trace may have branches or vias which makes accurate measurement very difficult
* Adding extra pads and vias for testing on the PCB will affect the performance of the controlled impedance trace and will occupy space needed for the function of the PCB.

Test Coupons

The typical test coupon is a PCB approximately 200x30mm with exactly the same layer and trace construction as the main PCB. It has traces which are designed to be the same width and on the same layer as the controlled impedance traces on the main PCB.

When the artwork is produced, the same aperture code (D-code) used for the controlled impedance traces is used to produce the test traces on the coupon. Since the coupon is fabricated at the same time as the main PCB the coupon's traces will have the same impedance as those on the main PCB. All planes are included on the coupon and they are interconnected on the coupon only, to ensure that test results are valid. It is necessary to include a void around the coupon on the reference planes so as not to affect the connectivity of the PCB itself if BBT (Bare Board Test) occurs whilst still on the panel.

Usually one coupon is made at the end of each panel to ensure that the coupon is representative of the whole panel i.e. testing the 2 coupons will verify to a high confidence level that there are no differences in trace width, trace thickness, laminate height, etc. over the whole panel. In fact some customers use the measurement of controlled impedance traces on test coupons on each panel to check the overall quality of PCB manufacture even when the PCB contains no controlled impedances. Since the coupon's controlled impedance depends on all the PCB parameters, it is a very accurate measure of consistency of manufacture without sectioning the PCB.

In addition to the usual PCB specifications, the PCB designer should specify:

* Which layers contain controlled impedance traces
* The impedance(s) of the trace(s) (there can be more than one value of impedance trace per layer)
* Separate aperture codes for controlled impedance traces e.g. 4 mil non controlled impedance trace and 4 mil controlled impedance trace.
* And either:

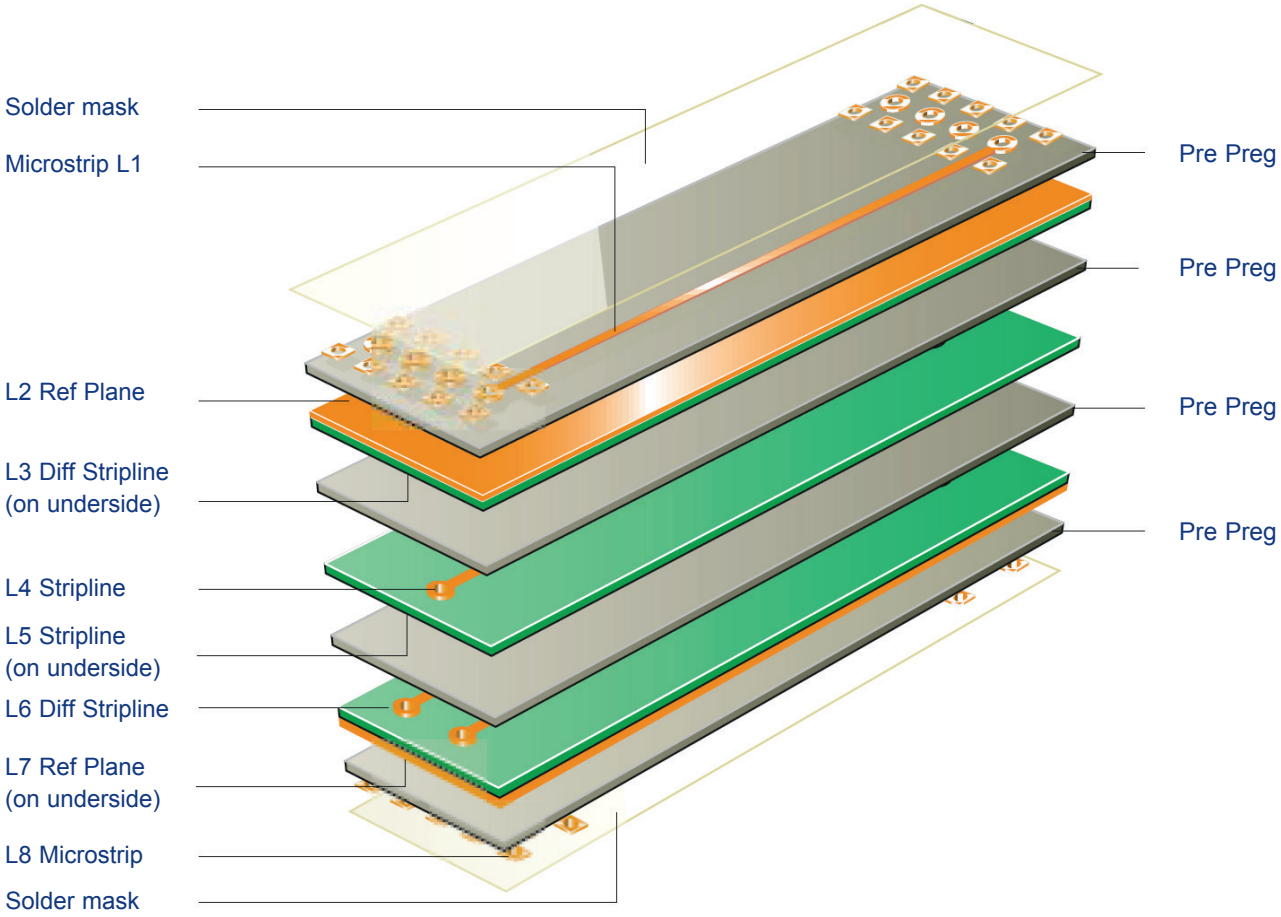
1. the width (w) of the controlled impedance trace or
2. the laminate thickness (h) adjacent to the controlled impedance trace

In case 1, where trace width (w) is specified, the manufacturer will adjust the laminate thickness (h) to give the correct value of impedance. In case 2 where the laminate thickness (h) is specified, the manufacturer will adjust the trace width (w) to achieve the value of impedance. In all cases it is advisable for designer and fabricator to discuss the possible solutions to ensure a cost effective and manufacturable stackup.

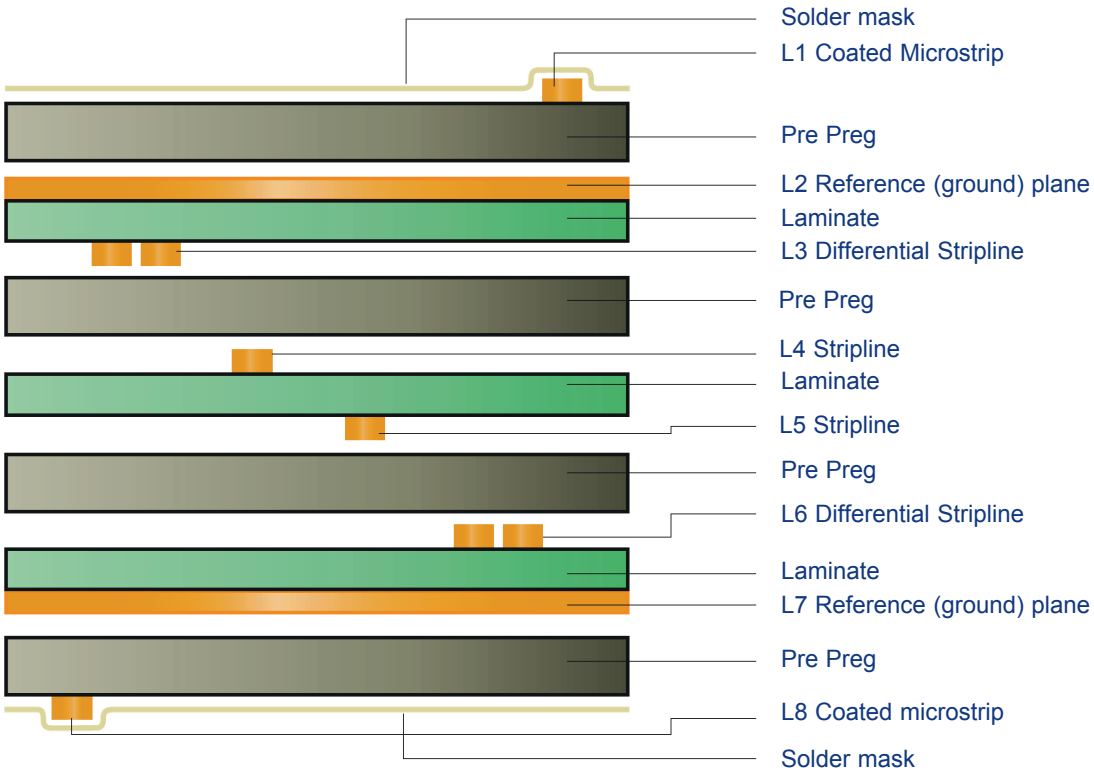
Some configurations (differential, coplanar) may have more than one parameter that can be varied to obtain the specified impedance.

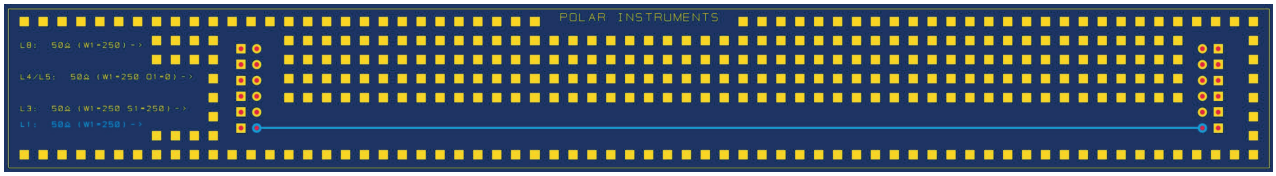
If you are designing or manufacturing high layer count PCBs,or simply have a high number of impedance controlled traces to document it is beneficial to use layer stackup design tools such as Polar Speedstack - possibly in conjunction with impedance coupon design tools like CGen.

Exploded view of a test coupon

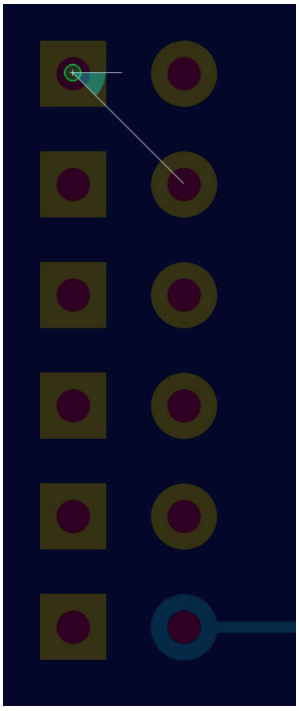


Exploded view of a test coupon





Coupons are easy to generate with a coupon generator like CGen which can take input manually, or from Speedstack or Si8000m field solver with Projects.



Typical Test Coupon

1. Dielectric separation will replicate impedance structure on printed boards.
2. Test connection holes shall be plated through to access all inner layer test conductors.
3. Square pads identify plated through hole connections to access all ground/power reference planes.
4. Conductor widths will replicate critical conductors on each impedance layer.
5. Via holes to be added as required.
6. Thieving to be added to outer layer as required.
7. Two coupons per panel assists in process control. These to be individually identified respectively.
8. Job No. + Datecode to be added as per customer requirements.
9. All planes to be interconnected (on test coupon only).

Capacitive loading

To minimise capacitive loading during test, you should minimise the size of pads and vias on coupons, especially for high impedance traces.
A coupon design with pads at both ends, gives you the option to test for trace taper. If the trace rises from one end and falls from the other the line is tapered. If it rises when measured from either end there is dc resistance in the line and this needs to be accounted for with dc resistance compensation or launch point extrapolation before analysis with a field solver.

Calculating the value of impedance using field solvers and documenting stackups with layer stackup design tools.

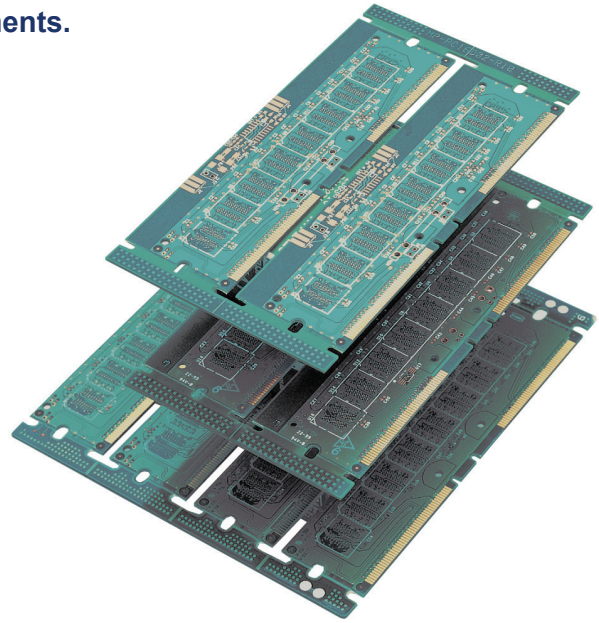
Simple published equations used to be adequate to obtain the nominal values of trace dimensions for a particular impedance and they were reasonably effective for line widths and spacing above 15 mil (thousandths of an inch). However these simple equations are only approximations and do not give accurate results for line widths used on current technology PCBs.

You will need to use Field Solver software for calculation of PCB controlled impedances. Their effectiveness is enhanced if they offer “goal seeking” that lets you enter the desired impedance and the field solver calculates the trace dimensions.

If you are working on thin copper and fine line designs (sub 4 mil) you may need to set the measurement system to remove any dc resistance effects from the measurement before goal seeking and correlating results.

Polar Instruments produces Field Solver software specifically for the prediction of PCB trace impedances based on trace configuration, trace geometry and material characteristics. There are two alternatives, the base model solver which calculates characteristic impedance, and a frequency dependant solver for traces working over 2GHz where you may also need to account for insertion loss.

To see Polar solvers in action please contact us (find contacts at **polarinstruments.com**) or watch the introductory videos on the Polar YouTube channel **www.youtube.com/polarinstruments.**



Using Field Solver software is a good starting point for obtaining nominal values of trace width (w) and laminate thickness (h) to obtain specific values of impedance. However if you are a fabricator moving to impedance control for the first time you will need to produce test panels containing many coupon designs, with different trace widths, different configurations (Stripline, Microstrip, Embedded Microstrip) and different layer structures with different laminate / pre-preg thicknesses, in order to get familiar before quoting on live jobs.

Ideally you will produce standard coupons (see suggested design) and each coupon can contain a variety of different impedances.

After manufacture of the test panels, you will then need to measure the actual values of impedance and see how they correlate against theoretical values. Laminate suppliers will provide you with lists of Er (dielectric constant) for different core constructions, typically FR4 has Er approximately equal to 4.2.

Since first writing this book the number and types of laminates supplied for specialist purposes (high reliability / low loss / aerospace / automotive) has proliferated, and using layer stackup design software like Speedstack with its link to online material libraries will greatly speed the process of stackup design.

By constructing a table of results comparing the measured values with the calculated values, you will see the variance between your process and the theoretical calculations. You can then remake the test panels, altering (w) and / or (h) to obtain the “exact” design values of impedance.

After several iterations, you will have an understanding of your process that allows you in most cases to take the designer’s requirements and convert them into values that suit your process and produce boards whose impedances are centred around the specified nominal impedance to maximise yield.

It is also useful to microsection some of the coupons to verify the actual dimensions of the traces compared to the nominal values.

These measured dimensions can be used in the equations to calculate an impedance value from the actual dimensions, adding a third column to your table of results.

We should mention that the presence of solder resist affects the impedance of surface microstrip and you should include this in your characterisation process.

Impedances typically range between 40 ohms to 120 ohms. The higher impedances are more difficult to control since they typically have narrower traces and will be relatively more affected by the exact etch process (i.e. since the impedance is inversely proportional to the trace width and thickness, as traces become very thin, the relative effect of the etching process will have a greater effect on their width and profile and hence, impedance).

The following relationships will give you an idea of how impedance depends on dimensions, however please remember they are only approximations for fine line widths:

- Impedance is inversely proportional to trace width
- Impedance is inversely proportional to trace thickness
- Impedance is proportional to laminate height
- Impedance is inversely proportional to the square root of laminate Er

Polar Instruments designs and manufactures rugged Controlled Impedance Test Systems specifically for PCB measurements in the manufacturing environment.

Polar is a world leader supplying instruments to premier PCB manufacturers around the globe.

Impedances can be measured using:

* A Network Analyser
* A laboratory Time Domain Reflectometer (TDR)
* A Controlled Impedance Test System (employing TDR techniques)

Both Network Analysers and laboratory TDRs are highly complex and sophisticated laboratory instruments that typically need to be operated with great care even by a skilled engineer. A Controlled Impedance Test System (employing TDR measurement techniques) that is specifically designed for measuring controlled impedances on PCBs offers the optimum solution. This is typically achieved using software to control the TDR and to acquire and process the data which it produces.

A TDR applies a very fast electrical step signal to the coupon via a controlled impedance cable and a specialised probe to connect to the pads on the coupon “launch pad”. Whenever there is a change in impedance value (discontinuity), part of the signal power is reflected back (as discussed earlier) to the TDR instrument which measures this reflected signal. The time delay between the transmitted pulse and the receipt of the reflected signal is proportional to the distance of the discontinuity. The magnitude of the reflected signal is related to the value of the discontinuity.

From this data it is possible to graph impedance versus its position on the test coupon. TDRs for production use are calibrated to have their accuracy focussed on impedance rather than time as the aim is to verify the fabrication process and not the circuit design.

A TDR specifically appropriate for the measurement of PCB controlled impedance in a manufacturing plant should be able to:

* Be operated reliably and conveniently in the normal plant environment by a non-technical person with minimum training requirement.
* Offer a degree of test automation for high throughput lines.
* Produce easy-to-understand results in the form of graphs of impedance versus distance over the length of the test coupon.
* Indicate and log unequivocal Pass/Fail results for each device tested.
* Datalog results and produce reports suitable for presentation to the customer.
* Store test files which contain the specifications for each type of coupon produced, and automatically set up the TDR.
* Be able to remove the effects of thin traces from the measurement with dc resistance compensation or launch point extrapolation.

Using airline standards

Precision airlines are accepted as the “standard” for controlled impedances. They consist of two accurately machined concentric tubes where all of the dimensions are very tightly controlled, terminated with a suitable connector. TDRs used for impedance measurement are precision measurement instruments and need to be regularly calibrated.

Reference air line standards are used for TDR calibration and are available in a variety of standard impedances (typically 28 Ohms, 50 Ohms, 75 Ohms and 100 Ohms).

Precision air lines are high cost metrology items and it is important to have your test system returned to an authorised service center for calibration annually against these standards.

Air lines are made traceable to National Standards (NIST, NPL) by a precision metrology technique called air gauging which allows the bores of the air line to be measured and the impedance calculated using a standard formula.

Many designs use a differential pair of traces between components. When compared to a single line trace (single ended), differential configurations are less susceptible to interference from adjacent traces and generate less interference.

To be effective, they need to be matched i.e.:

- Both traces should have the same dimensions and spacing to adjacent traces and planes
- The traces should be as close as possible to each other as the manufacturing process allows
- The spacing between the two traces should be constant

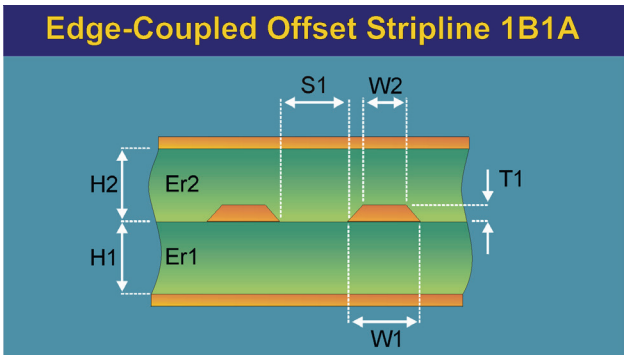
The value of the characteristic impedance depends on the trace separation as well as the dimensions of the individual traces and when you are measuring them, you will need to make a differential measurement. Typically the differential measurement will be slightly less than twice the value of the impedance of each trace e.g. if you measure each individual trace of a 100Ω differential pair, they are both likely to read around 53Ω or 55Ω.

Differential pairs operate with a positive signal on one line and a negative on the other. Depending on how close or far apart they are some of the return current will flow back to the probe via the underlying plane (100% if they are far apart) that's why there are 3 (2 signal and a ground) or 4 pins (2 signal and 2 ground) on a differential probe.

In some specialist applications there is no plane adjacent to the pair. (Under ethernet connectors for example). Polar has specialist probes with internal circuitry to measure these "groundless differential" traces. Microwave engineers would call these "balanced lines" as all the outbound current returns in the return side of the pair.

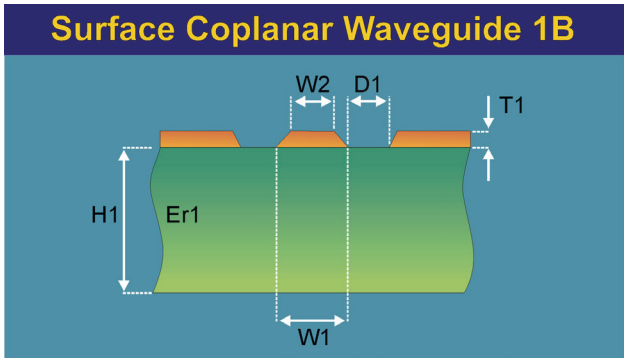
If you would like to learn more and why you should really think in terms of return current rather than ground it is worth investing in Dr. Eric Bogatin's comprehensive book:

"Bogatins Practical Guide to Transmission Line Design and Characterization for Signal Integrity Applications"

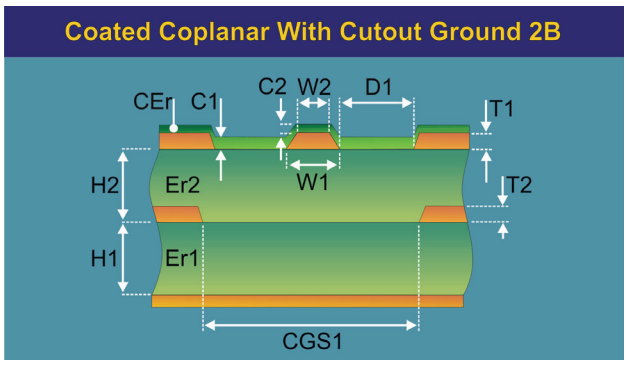


Coplanar configurations have become increasingly popular in the past few years. One of the benefits of surface coplanar configurations is that they extend the operating frequency of FR4 laminate, which loses performance above 2Ghz. In surface coplanar, most of the field between the trace and plane is through air rather than the laminate and so the loss caused by the laminate has less effect at high frequencies.

There are many useful variants of coplanar configurations. For example using a surface coplanar waveguide can make a flex impedance controlled circuit more flexible because the return paths are on the same layer as the signal. Traditional return paths on the layer below or above will create a virtual mechanical stiff I-beam which is difficult to fold. The coplanar line also has better high speed behaviour than the use of crosshatched ground planes.



On thin multilayers it can be necessary to reference to a plane below the immediately adjacent one in order to keep the trace width a reasonable size to manufacture. For this purpose the coated coplanar with cutout ground can show how wide the cutout needs to be “to keep it out of harms way”.



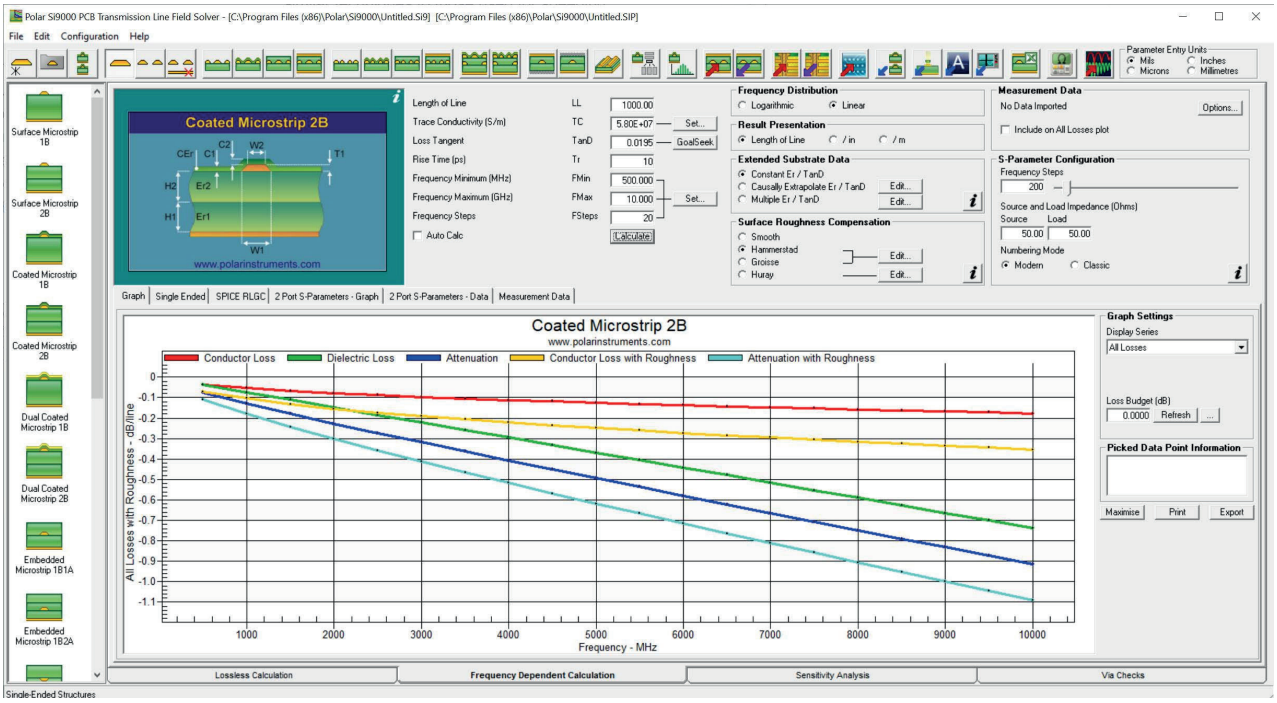
As speeds increase above 2GHz to 5GHz losses in the laminate (dielectric loss) progressively in the laminate rob the signal of its power turning the signal into heat in much the same way materials heat in a microwave oven. Likewise electrical effects force the current to travel only on the outer surface of the copper trace (“Skin Effect”)”. Effective resistance increases, which further dissipates power.

A designer can approach control of insertion loss in a number of ways. For instance simply keeping the traces short reduces insertion losses because it is proportional to length. Lower loss laminate materials may be chosen albeit at higher cost, and also smoother copper which mitigates the effects of roughness when all the current is travelling on the surface of the trace.

As you can see the drivers for loss are quite different from those for impedance, and the use of smooth copper may mean a fabricator needs to change processes to avoid the risk of delamination.

Unlike in lower speed designs the silicon in ultra high speed communications can also deploy pulse shaping on both the transmit and receive side of the circuits, using similar techniques to those used for speeding up broadband connections on copper cables.

You may hear the terms “pre emphasis” and “equalisation” to describe this. Polar has field solvers and stackup tools which extend the capability beyond characteristic impedance to also model the insertion loss. Si9000e and Speedstack Si both offer these extended capabilities.



Q. My customer says I need to test their PCBs at 900MHz. Can I do this with a TDR based test system?

A. Yes, a TDR based impedance test system is suitable for testing over a wide range of frequencies. The parameters that determine impedance (laminate Er) do not vary significantly below 3 to 4GHz. So it is unnecessarily expensive and time consuming to do a single frequency test using a network analyser. Remember that characteristic impedance only changes slightly with frequency.

Q. My customer does not specify that I measure controlled impedances,what should I do?

A. A designer may think that by specifying the dimensions, the traces will automatically have the correct value of impedance. As explained earlier, each manufacturing process requires characterisation to ensure that the process is matched to nominal values produced by Field Solver calculations. Work in partnership with your board specifier customer and help them understand the need for test.

Q. How do I calculate the dimensions for controlled impedances on inner layers on my stack up?

A. You can ignore any layers that are beyond the planes either side of the trace being calculated. You only need to consider the laminate thicknesses either side of the trace to the nearest planes on both sides.You can think of this as the plane forming a shield either side of the trace. If you have many impedance controlled traces and high layer counts Speedstack will save you time and provide accurate documentation.

Q. Why are all of the impedance measurements on my coupon wrong but the dimensions agree with the Field Solver?

A. You may have forgotten to connect all of the planes to each other. This is necessary to obtain the correct values. Remember that this should be done on the coupon only and you should leave a void around the coupon to avoid these interconnections affecting bare board test if the coupon is attached. You should also check that the impedance test probe is oriented the correct way with the ground side connected to the return from the reference plane.

You can read and download a wide range of Application Notes from our website at

www.polarinstruments.com

Controlled Impedance Test Systems (CITS)

The Polar Instruments CITS controlled impedance test system has become the industry standard for use by non technical operators in manufacturing environments. It is also widely used by OEMs to verify conformance of incoming PCBs. CITS uses TDR techniques to measure controlled impedances and it automatically reports when a measurement is outside the specified tolerance. It automatically processes the data to produce a simple display of impedance versus distance.

All results and system set up data are automatically datalogged. Data can be easily exported to a third party database (eg for statistical process control). Test Reports can be produced suitable for supply to customers. High accuracy is assured as instruments are factory calibrated against precision reference airlines at 28, 50, 75 and 100 ohms, all traceable to National Standards. The CITS delivers excellent gage R&R results

Polar tools for Stackup design impedance & insertion loss modelling and measurement

Polar provides suites of tools for Stackup, Impedance field solving and measurement for both impedance and insertion loss controlled PCBs. Si8000m is a time proven field solver for modelling PCB characteristic impedance, and Si9000e extends capability for designs requiring insertion loss modelling. Dielectric behaviour, Copper roughness and skin effect are all modelled with industry standard methods. Speedstack PCB and Speedstack Si design tools work with Polar field solver engines to design accurate stackups, and generate documentation using data for real world materials available through the comprehensive Speedstack online libraries. Speedstack can output test files and test vehicle data to CGen for test coupon design, and to CITS for testing impedance. Polar Atlas completes the loop by providing specialist measurement of PCB insertion loss when linked to a suitable TDR or Vector Network Analyser.

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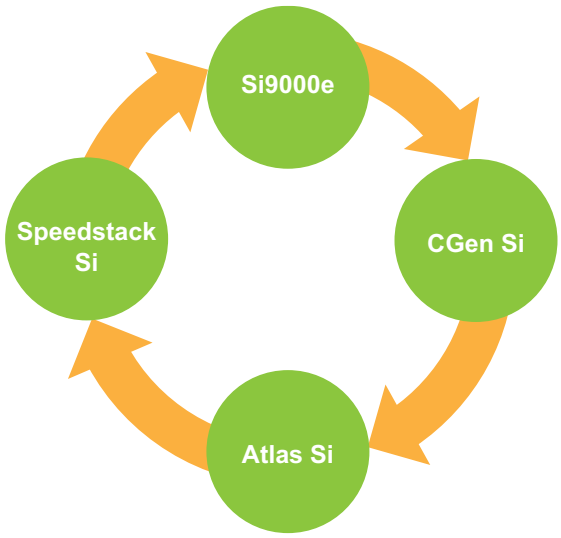

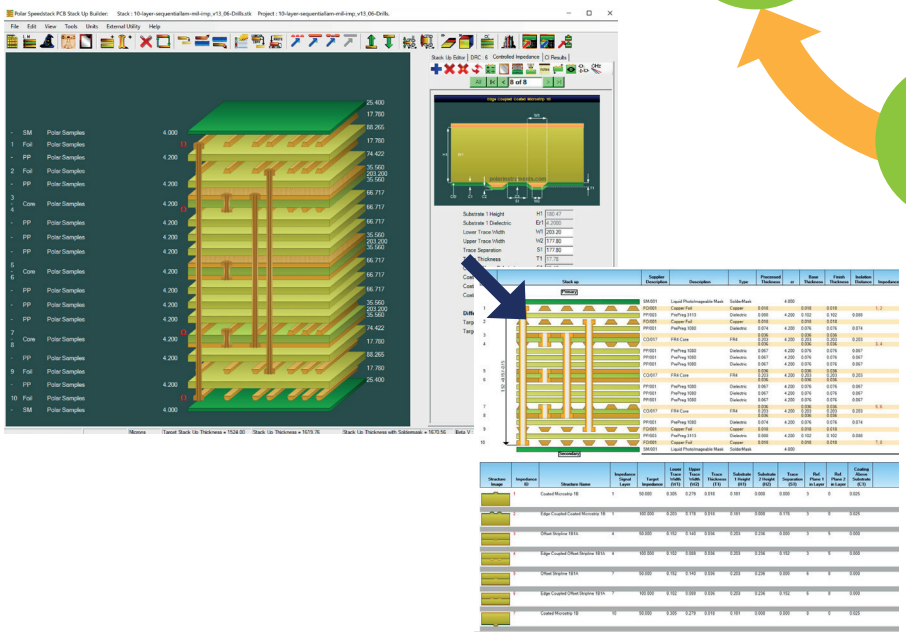

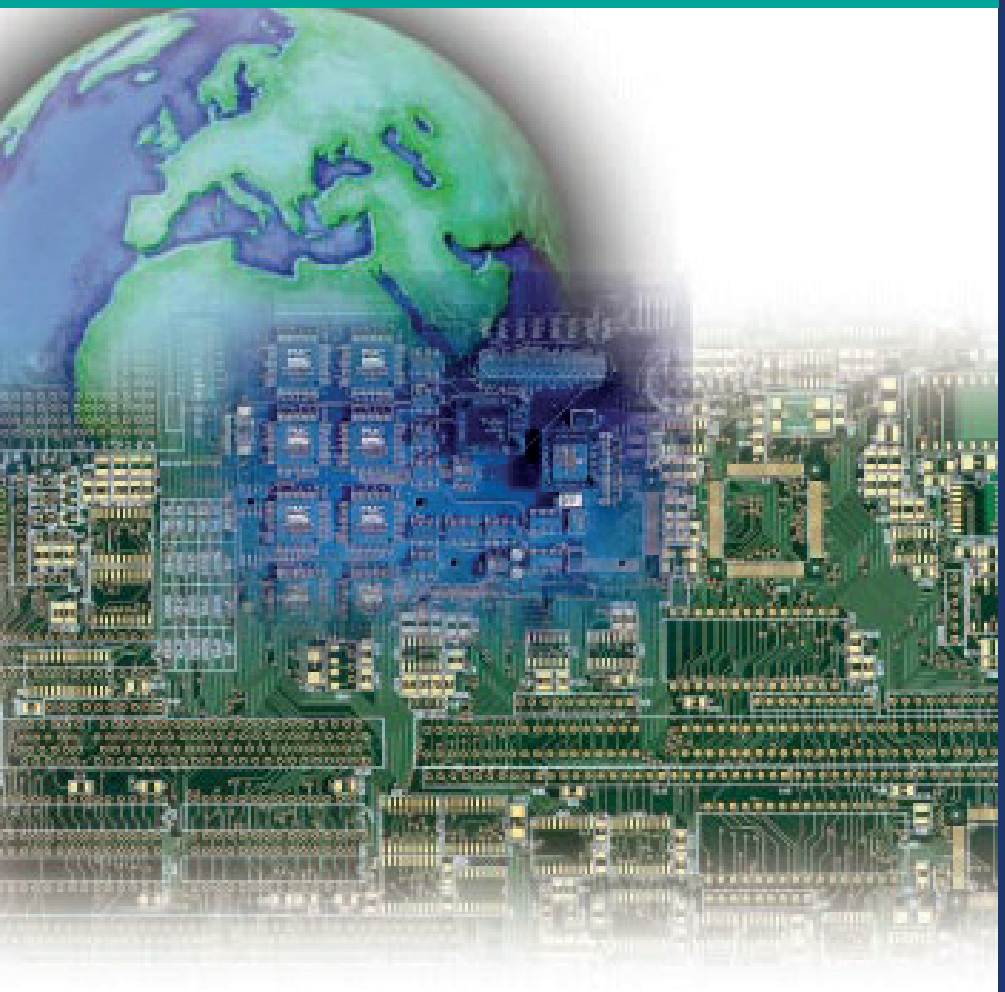

Polar Instruments

Established in 1974, Polar Instruments Ltd is recognised as a specialist designer & supplier of tools for the measurement and calculation of PCB controlled impedance and insertion loss.

Polar Speedstack stackup design software acts as the glue to join these comprehensive suites of tools and supply the links to 3rd party CAD CAM and registration tools. By focussing and specialising in this area, we are able to work closely with our customers to ensure that our products are continually enhanced to meet industry needs.

Polar is ISO90001 certified and we have world wide representation to offer the level of support that you require.

Further information along with contact details are available on our website:

polarinstruments.com

$32.50

Polar Instruments pursues a policy of continuous improvement. The specifications in this document may therefore be changed without notice.

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