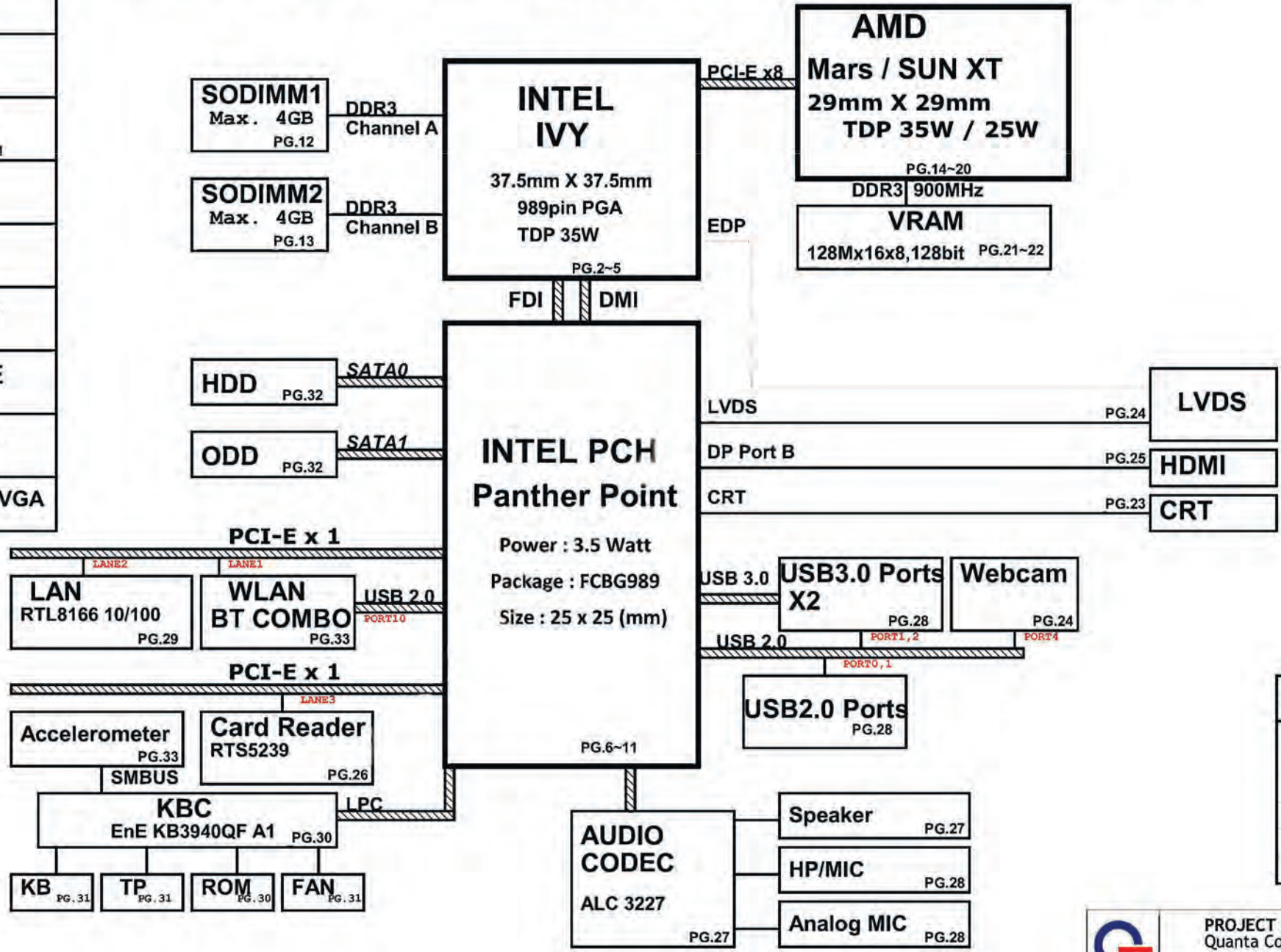
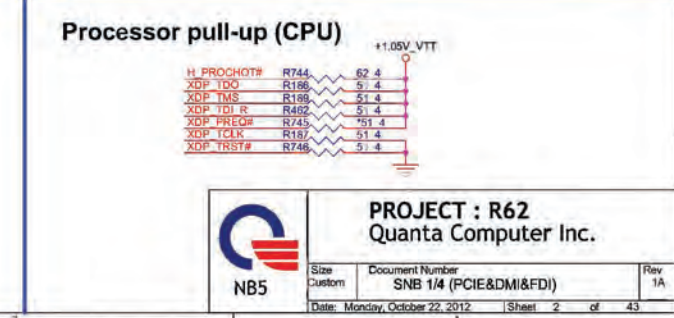
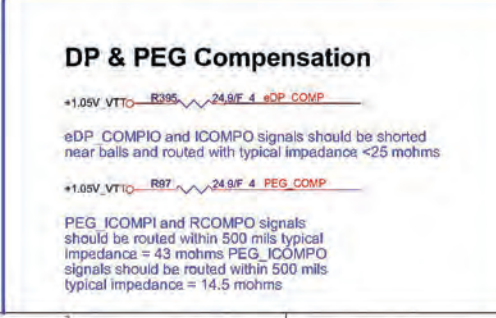
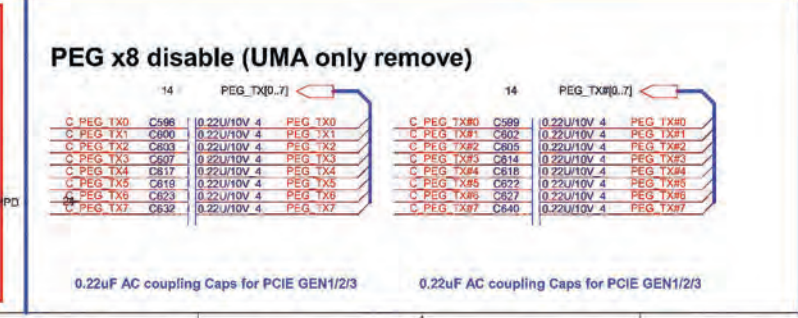
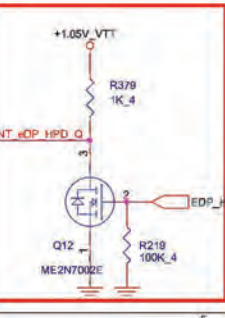
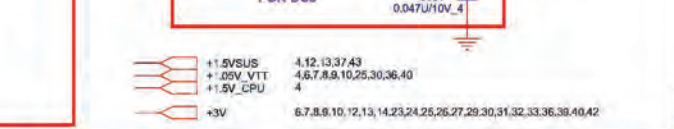
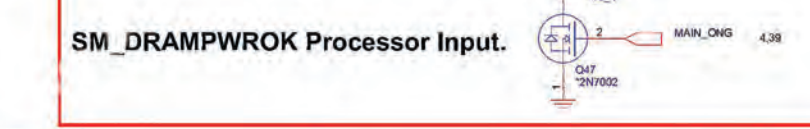
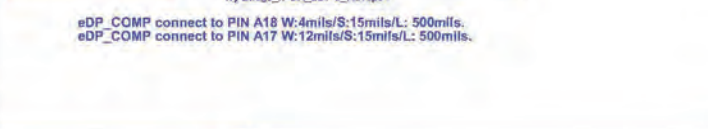
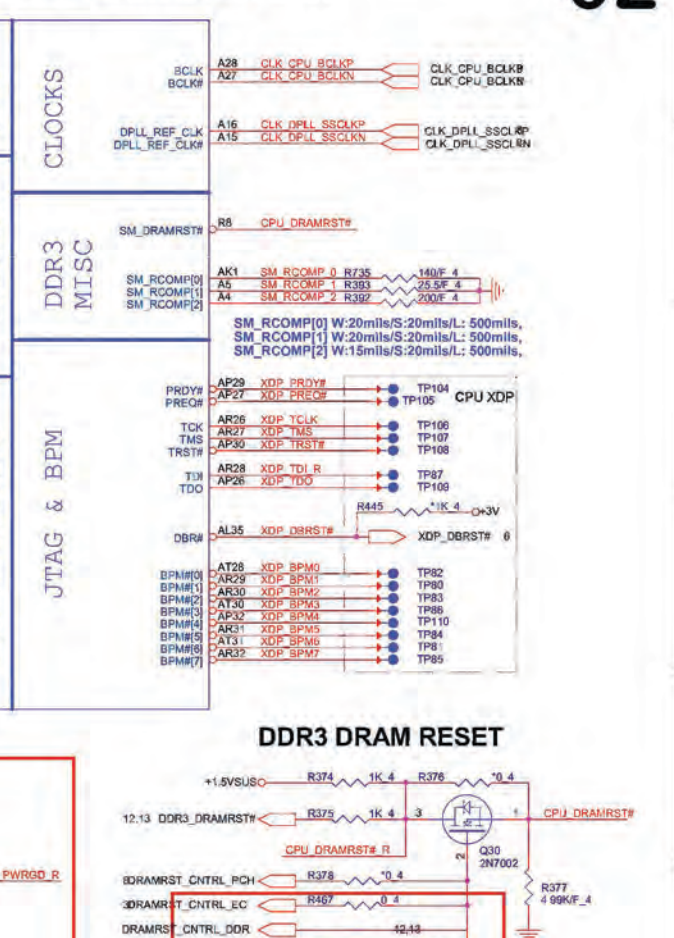
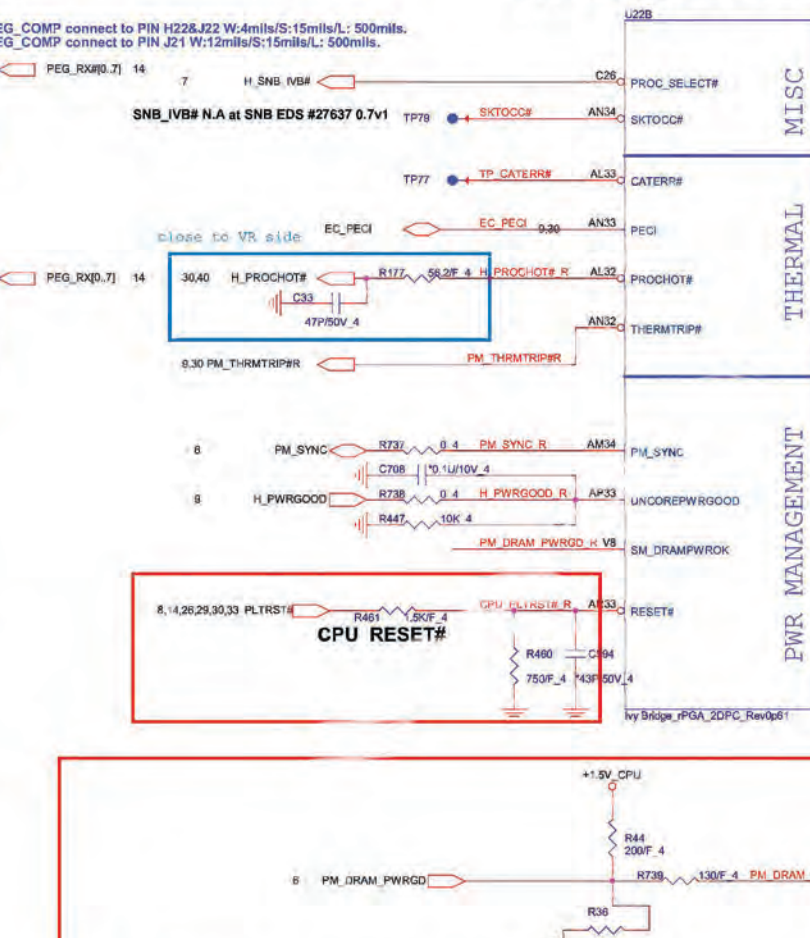
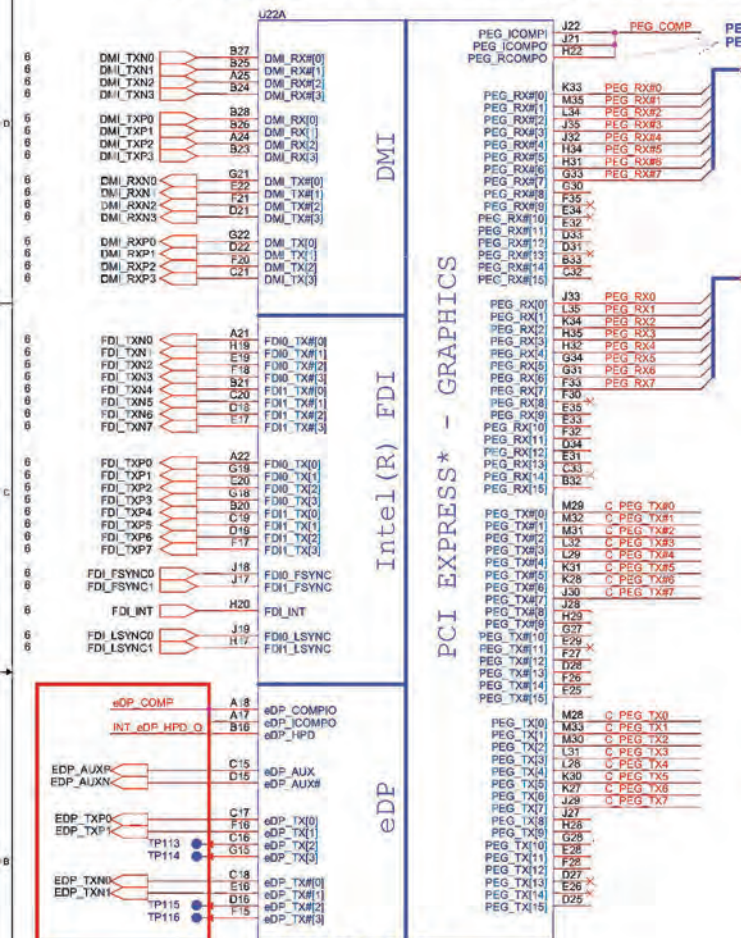


R62 INTEL CHIEF RIVER SYSTEM DIAGRAM

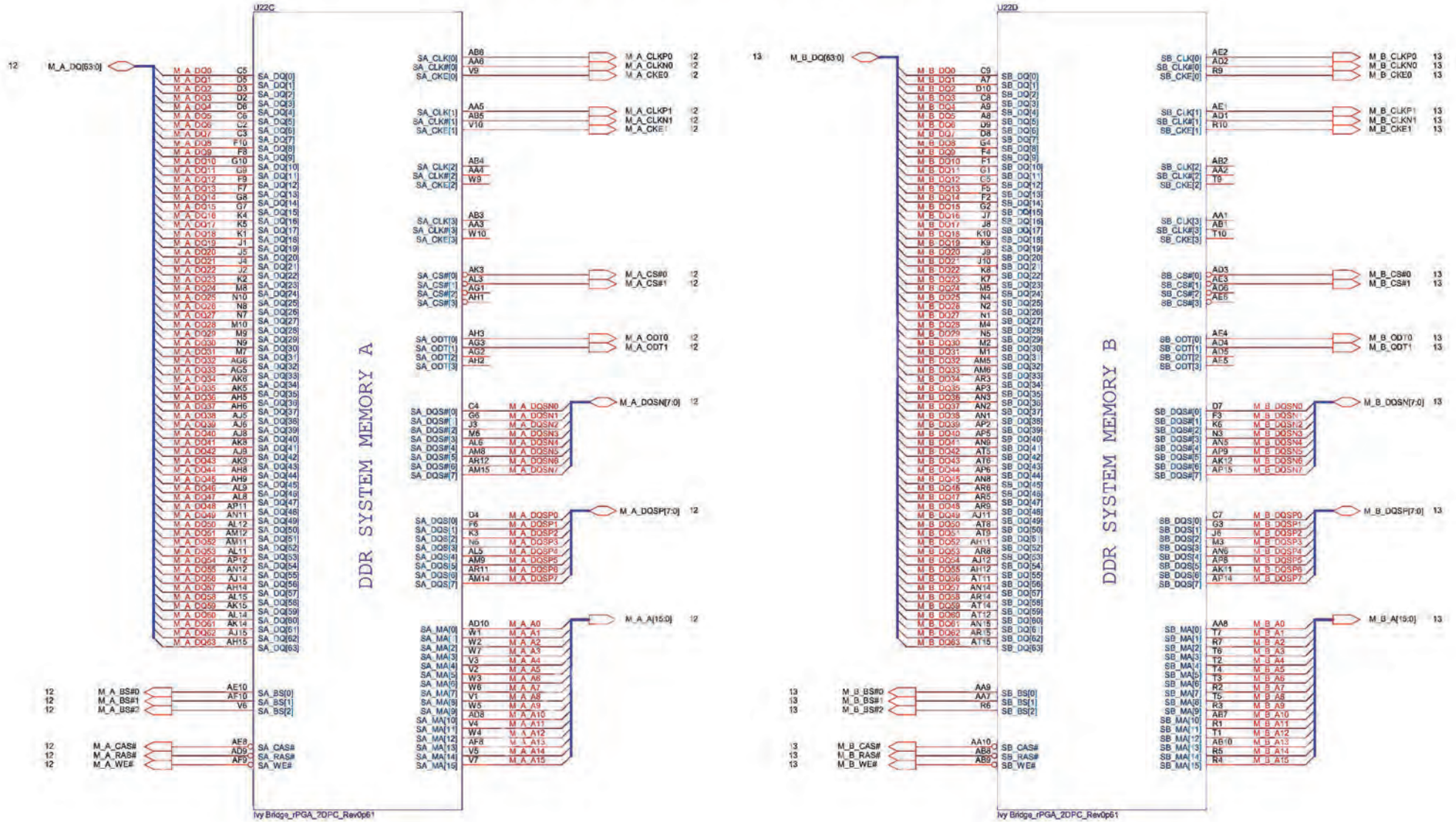
+3V/+5V S5
PG.35
+1.05V
PG.36
CPU Core
PG.40~41
DDR3
PG.37
Charge
PG.34
Dis-Charge
PG.39
+VGACORE
PG.42
+VCCSA
PG.38
+1.0V/+1.8/ +3 VGA
PG.43



Stackup
TOP
GND
IN1
IN2
VCC
BOT



Ivy Bridge Processor (DDR3)



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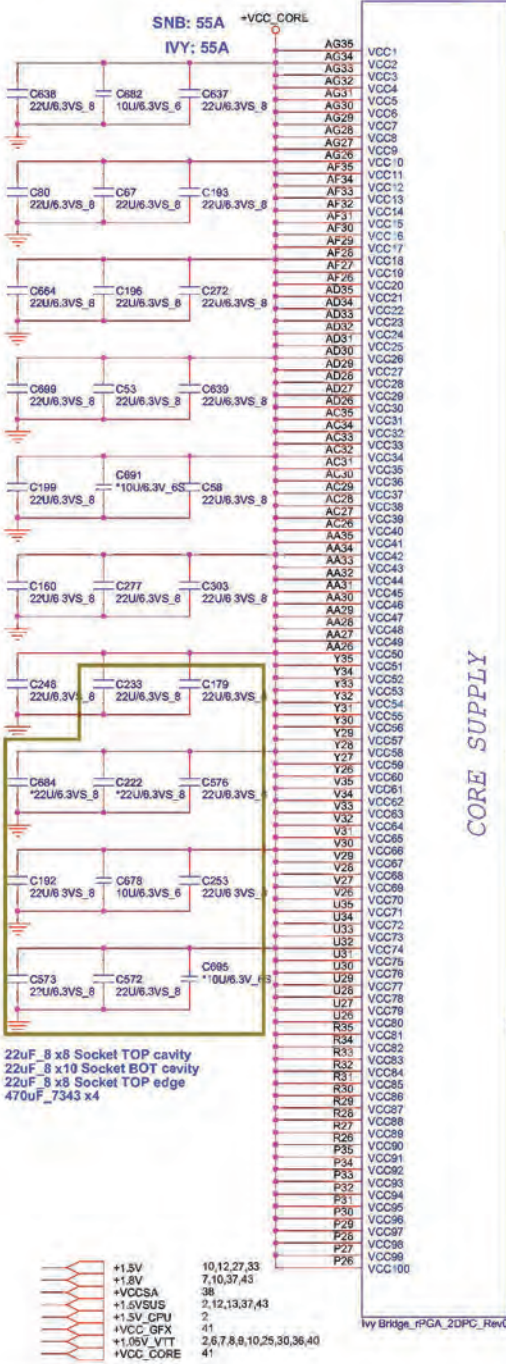
NBS

Rev 1A

Ivy Bridge Processor (POWER)

POWER

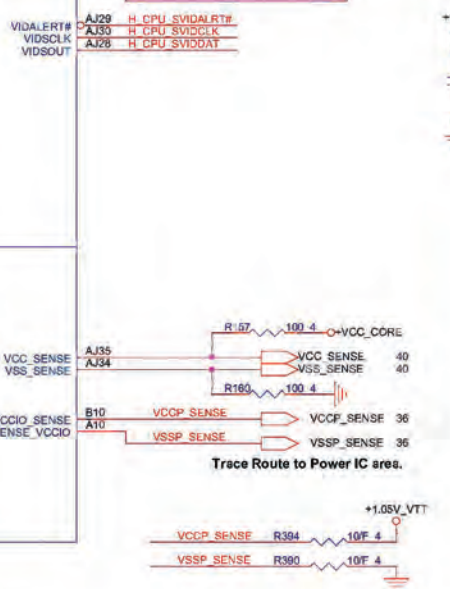
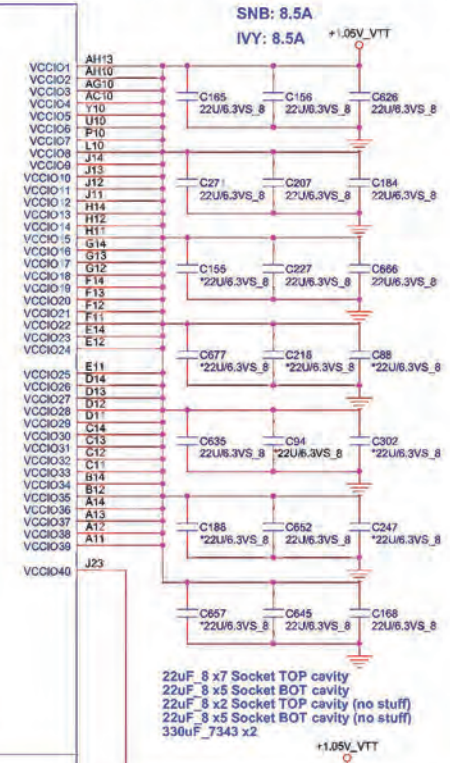
U22F



PEG AND DDR

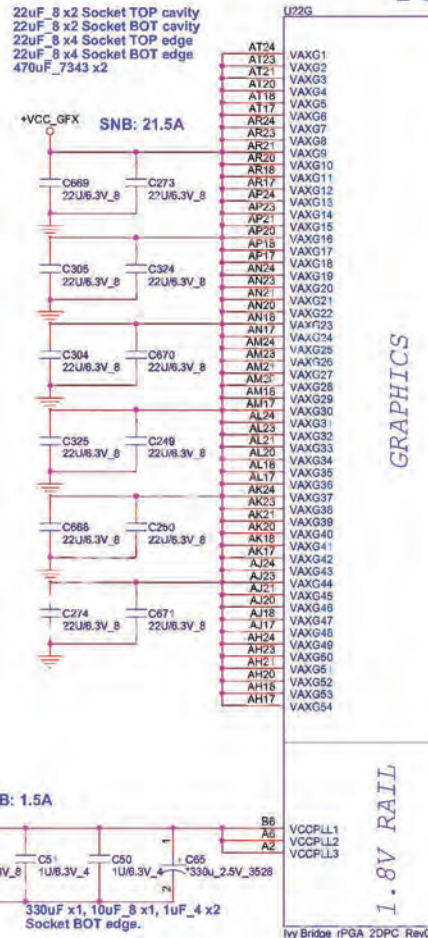
CORE SUPPLY

SENSE LINES



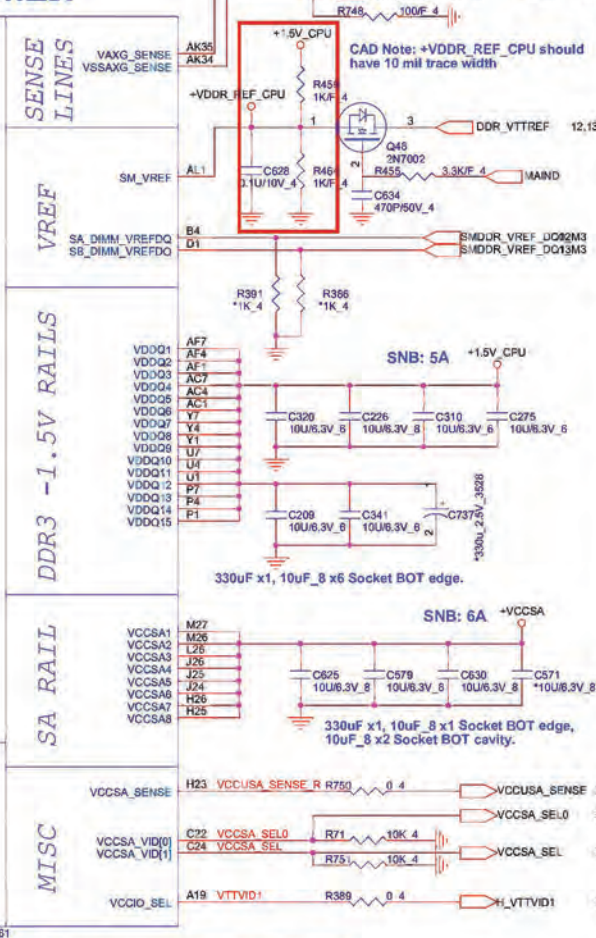
POWER

U22G

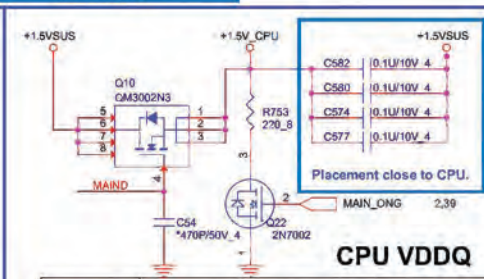
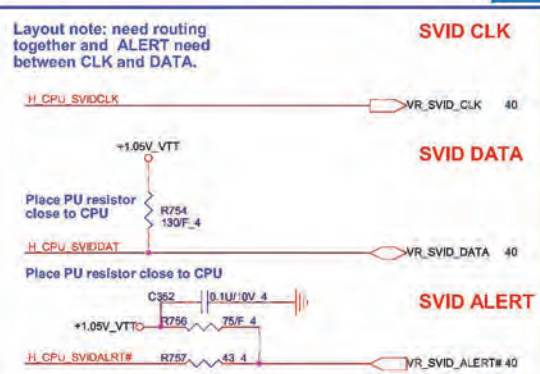


GRAPHICS

1.8V RAIL



04



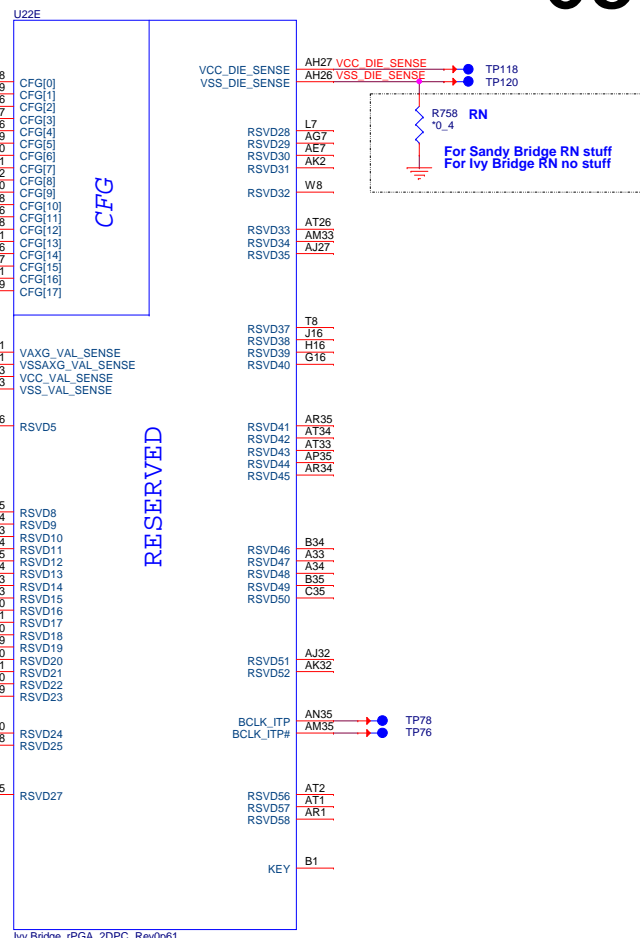
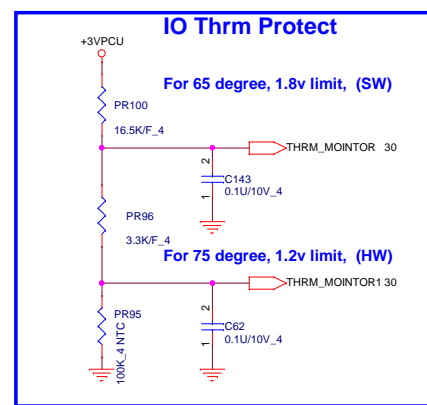
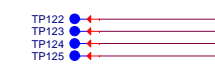
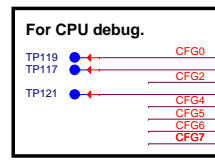
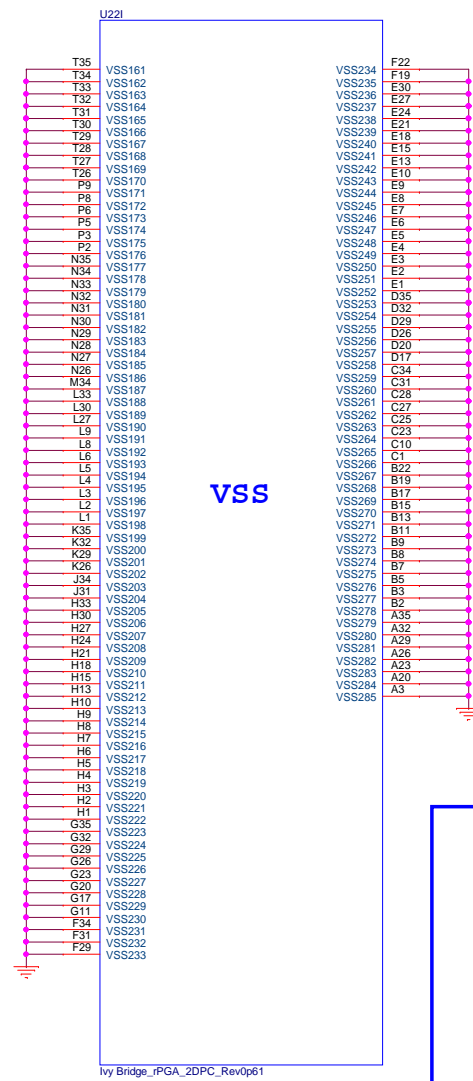
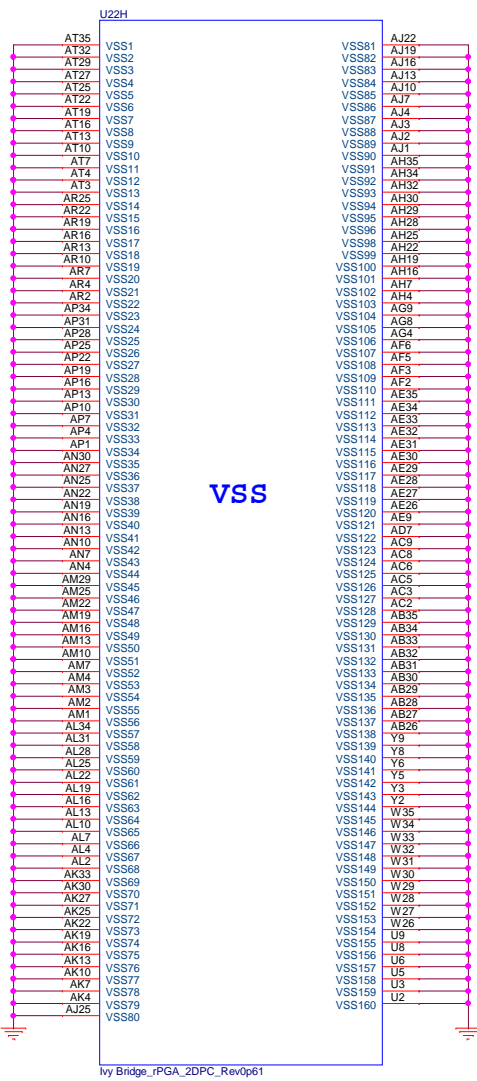
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NBS

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Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

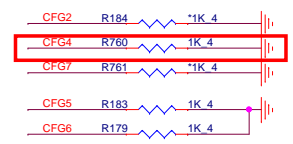


For rPGA socket, RSVD59 pin should be left NC.

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

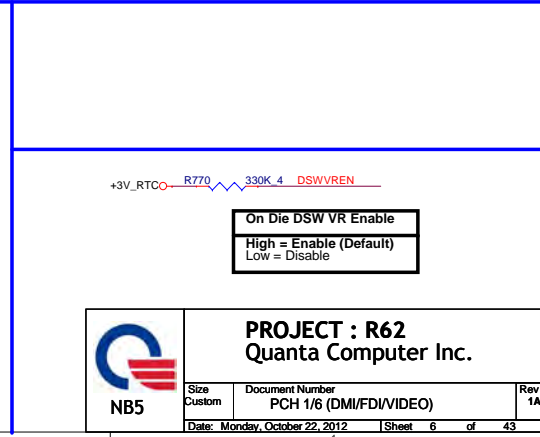
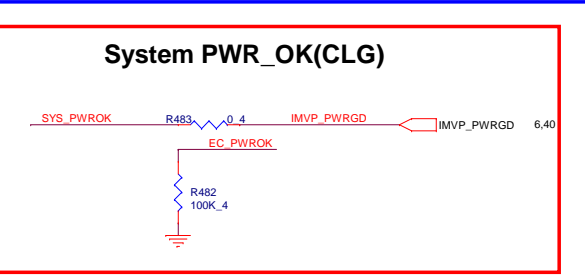
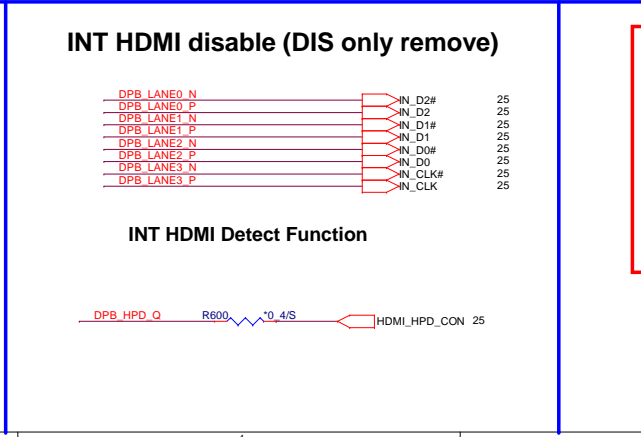
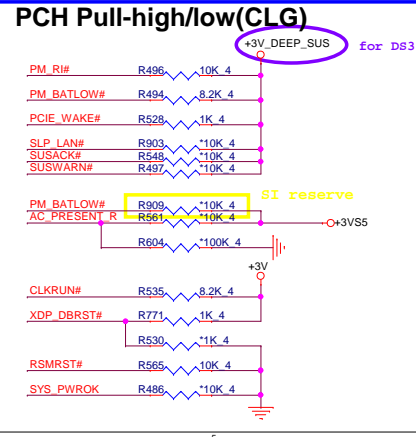
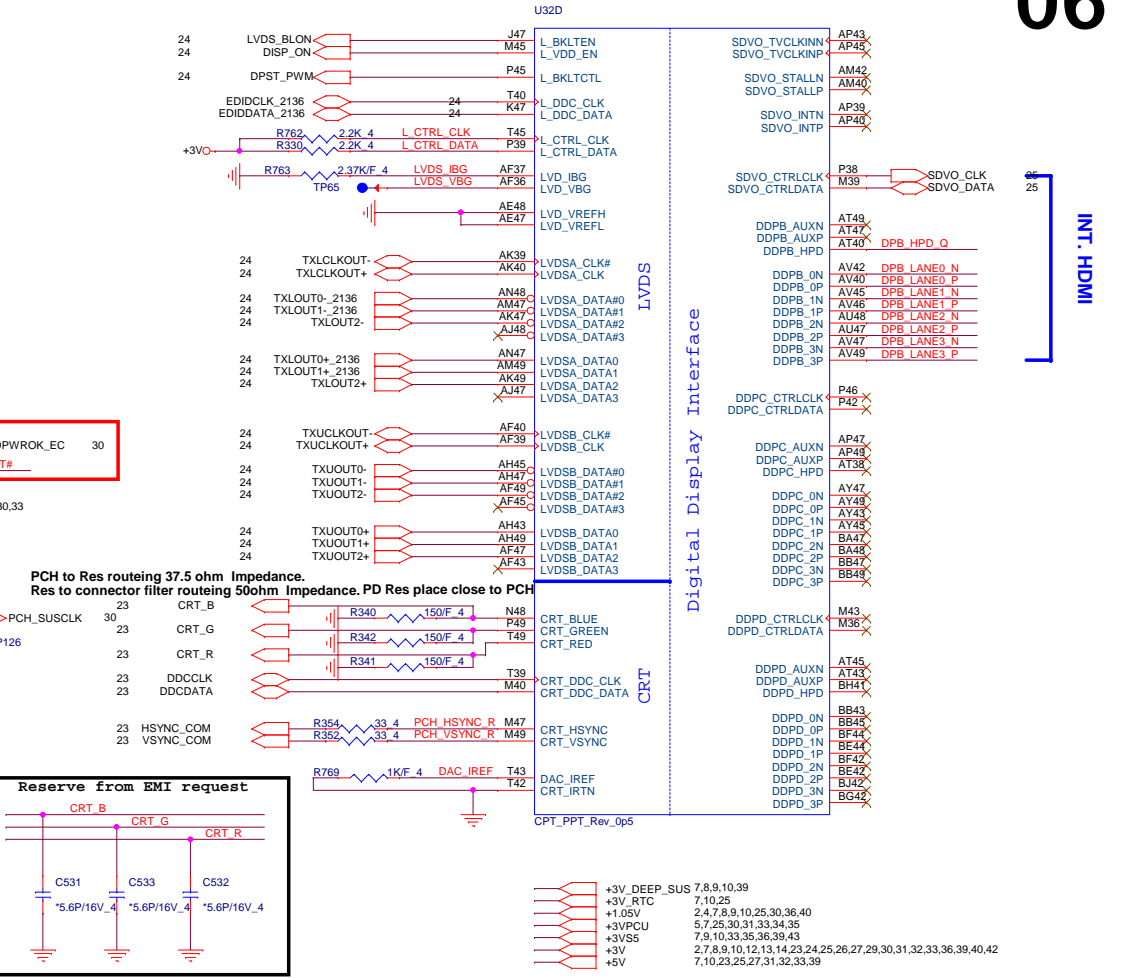
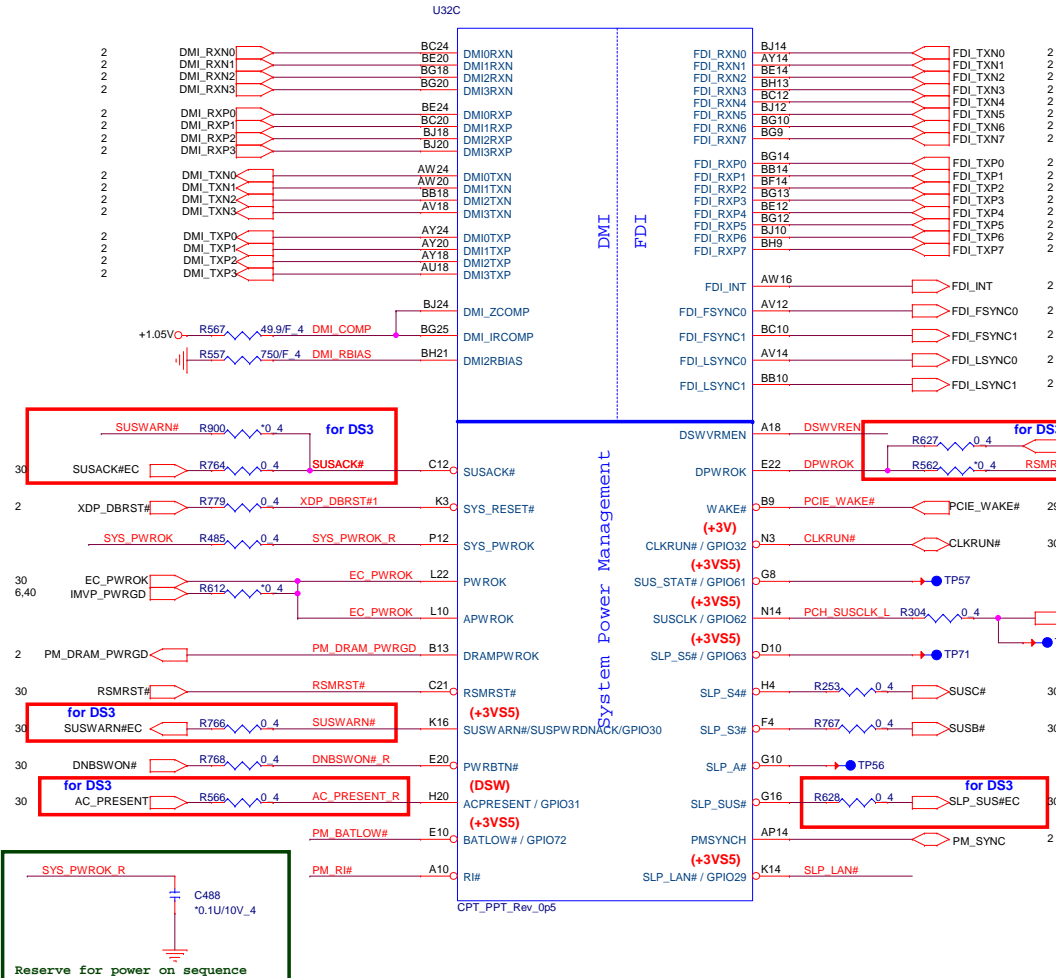
	1	0
CFG2 (PEG Static Lane Reversa)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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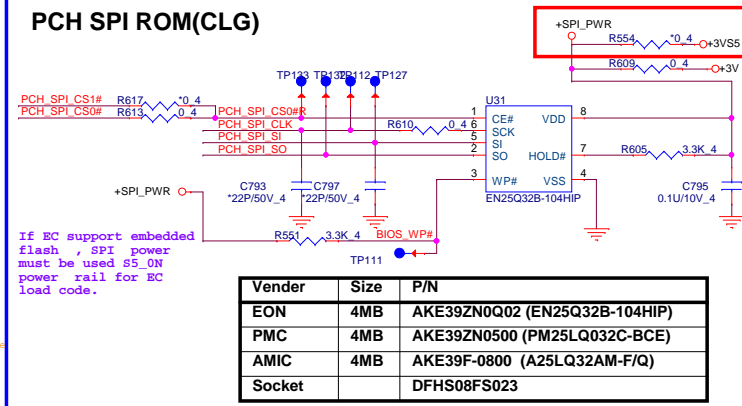
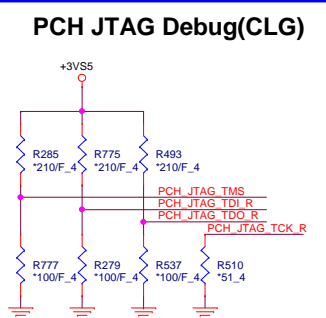
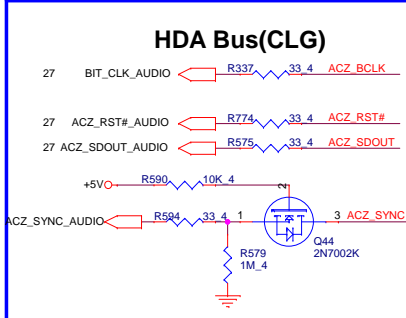
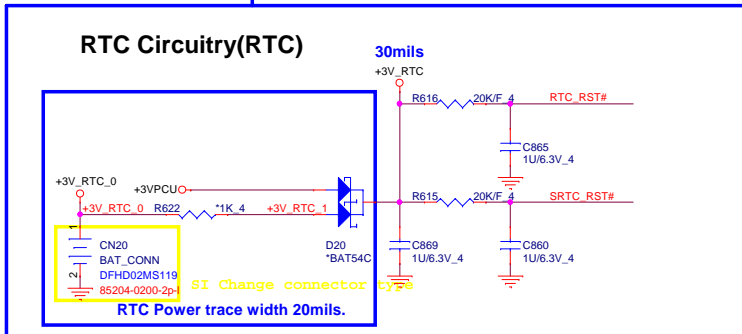
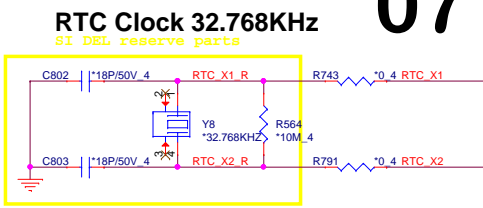
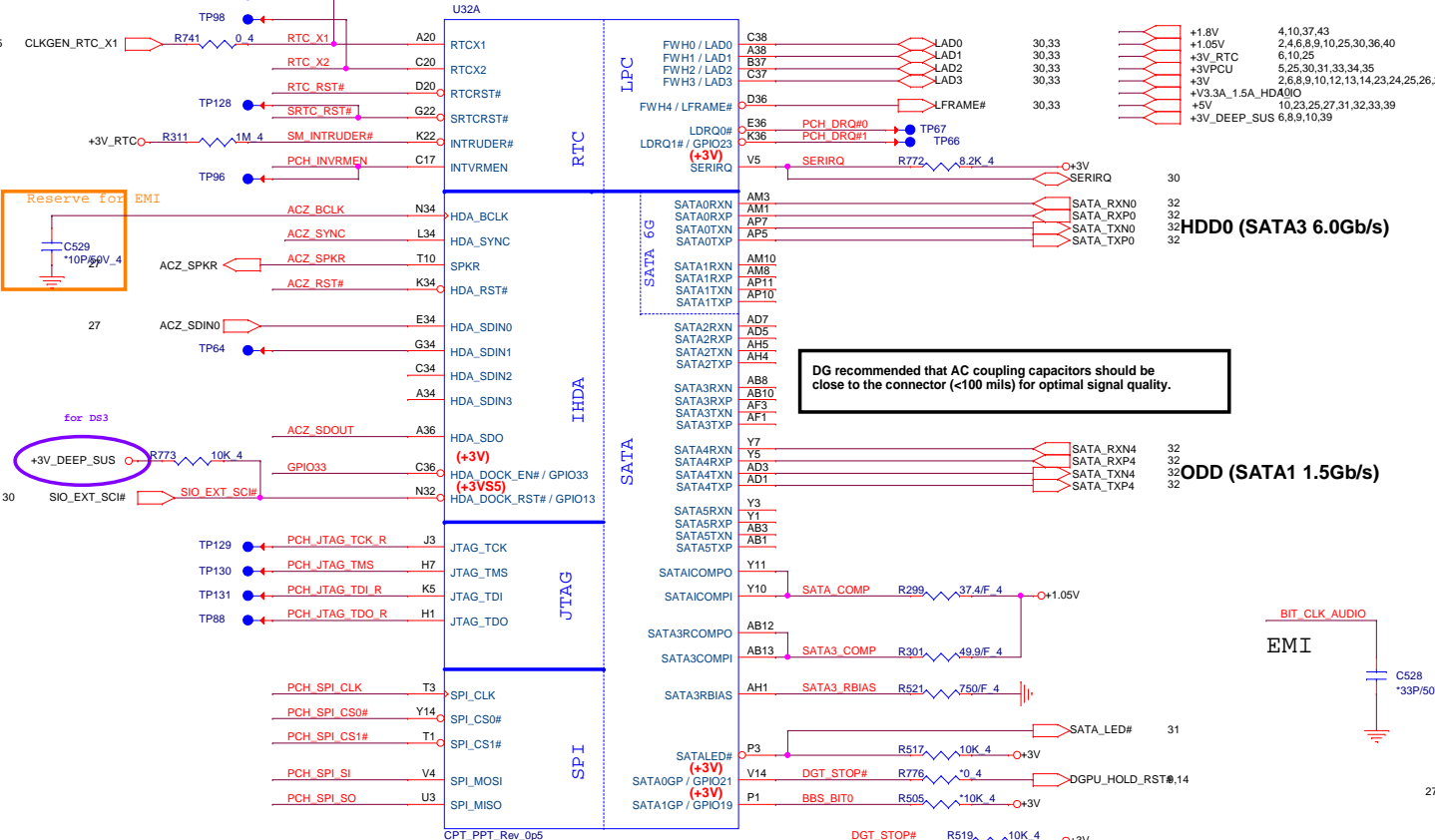


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Cougar Point/Panther Point (HDA, JTAG, SATA)



DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

ODD (SATA1 1.5Gb/s)

PCH Strap Table

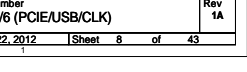
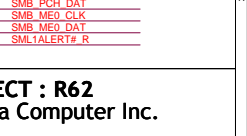
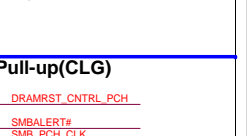
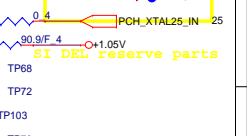
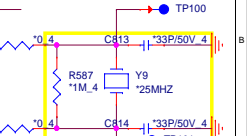
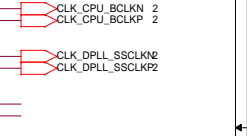
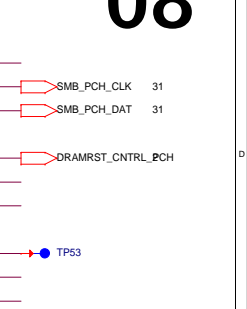
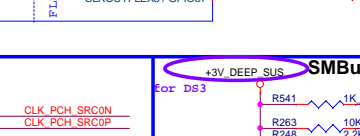
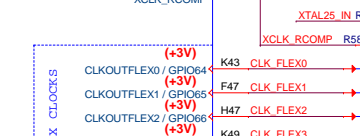
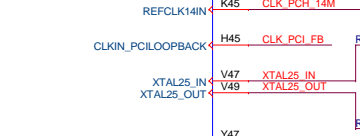
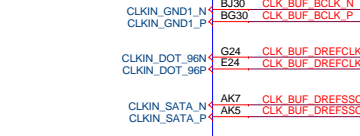
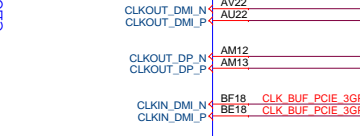
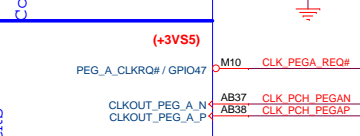
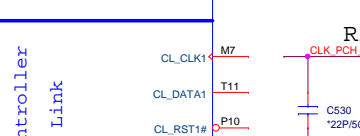
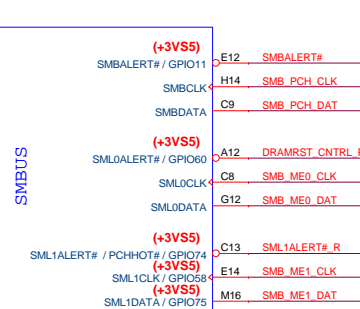
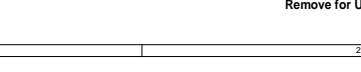
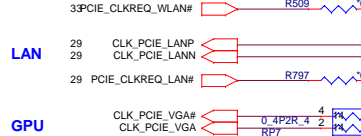
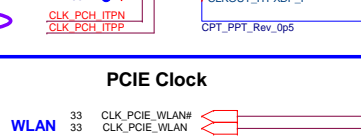
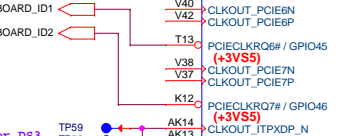
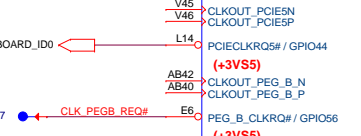
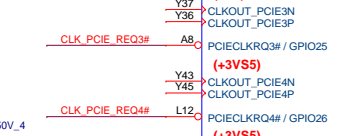
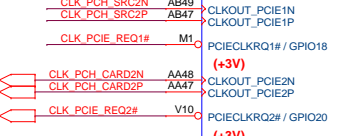
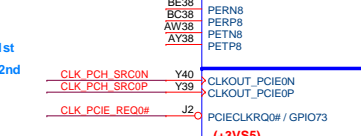
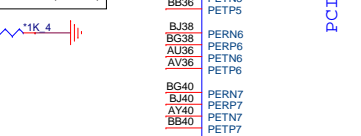
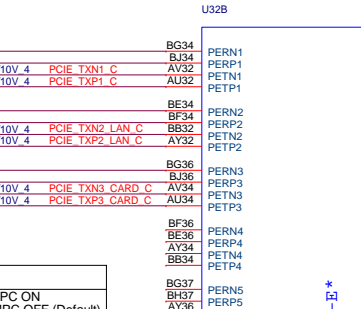
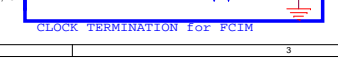
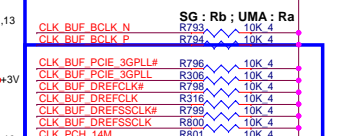
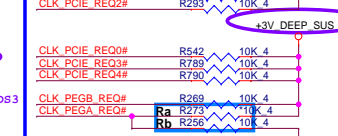
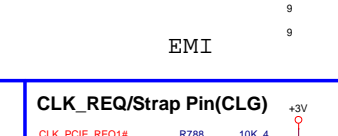
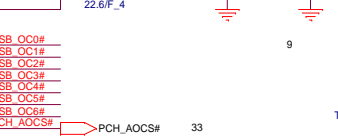
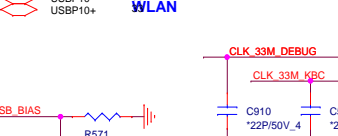
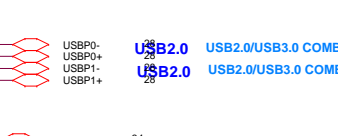
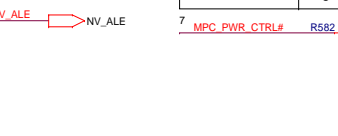
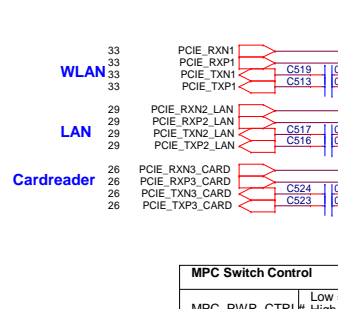
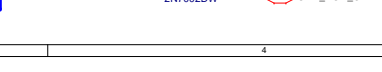
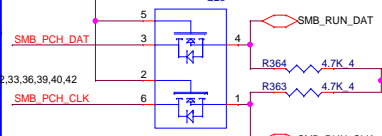
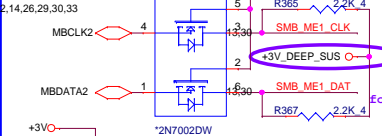
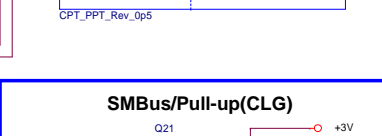
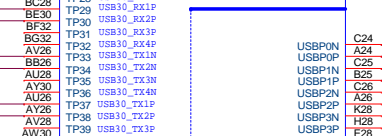
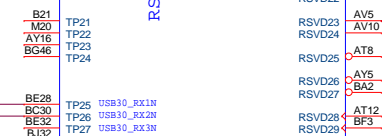
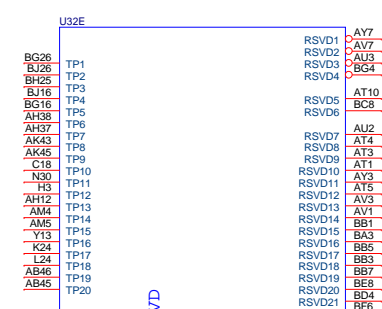
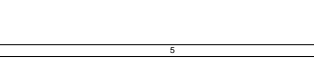
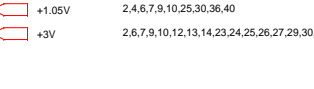
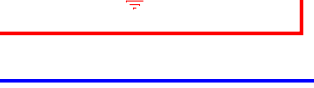
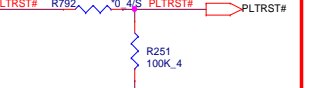
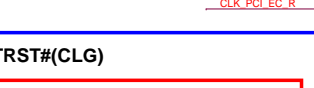
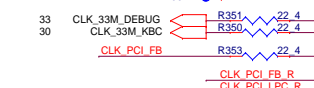
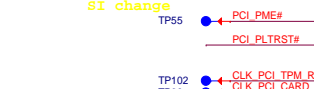
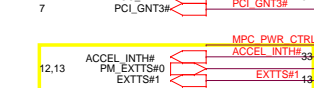
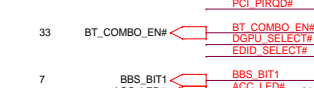
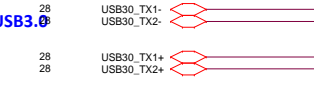
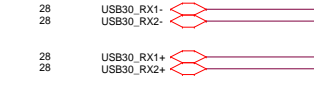
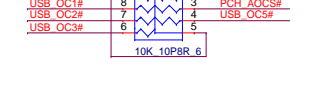
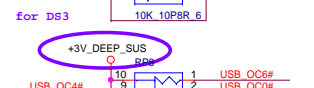
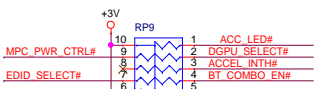
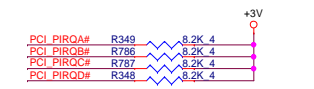
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V0 R595 10K 4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R572 0.4 2 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWR0K		R782 1K 4 R595 1K 4 BBS_BIT0 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWR0K	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWR0K	0 = Disable (Internal pull-down 20kohm)	+1.8V R783 1K 4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWR0K	weak pull-down 20kohm	+1.8V R526 2.2K 4 R546 1K 4 NV_CLE H_SNB_IVB# 9
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+V3.3A_1.5A_HDA_IO R784 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWR0K	0 = Default (weak pull-down 20K) 1 = Overriden	GPIO33_E ACZ_SDOUT R573 1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWR0K	0 = Default (weak pull-down 20K) 1 = Enable	

PROJECT : R62

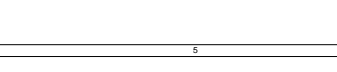
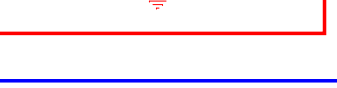
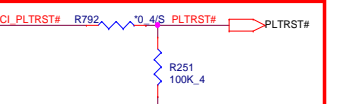
Quanta Computer Inc.

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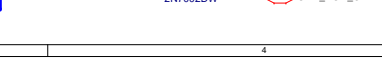
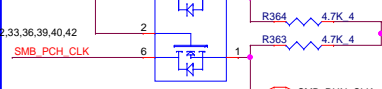
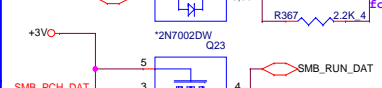
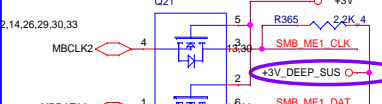
PCI/USBOC# Pull-up(CLG)



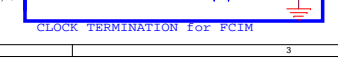
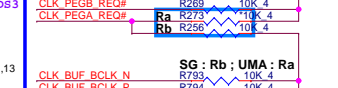
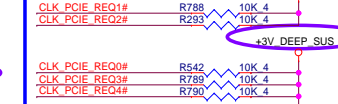
PLTRST#(CLG)



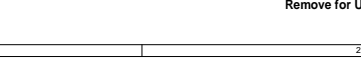
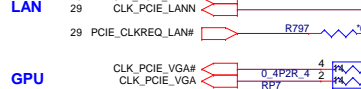
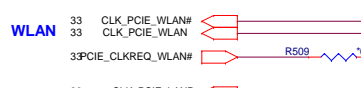
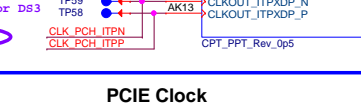
SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



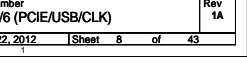
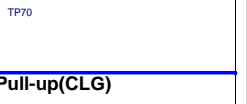
PCIE Clock



SMBus/Pull-up(CLG)

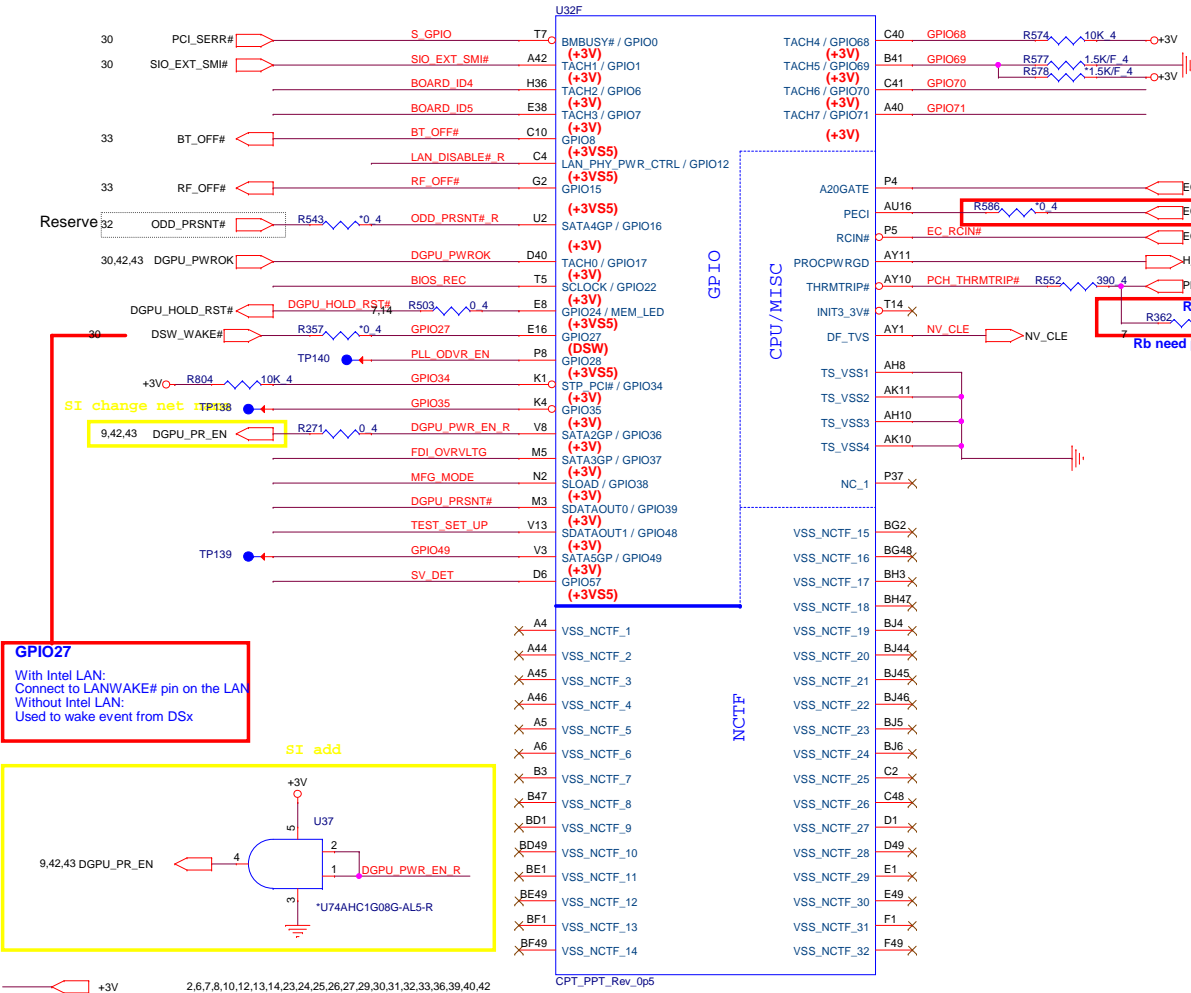


SMBus/Pull-up(CLG)

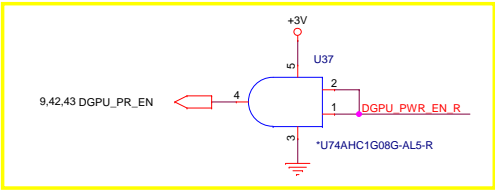


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Quanta Computer Inc.
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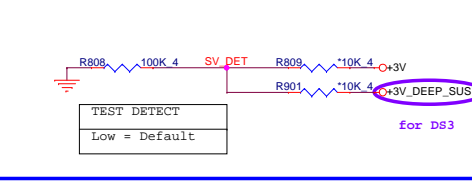
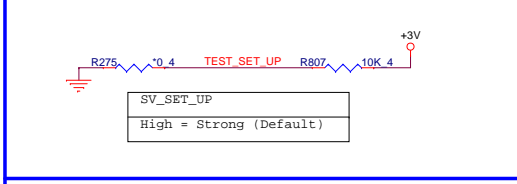
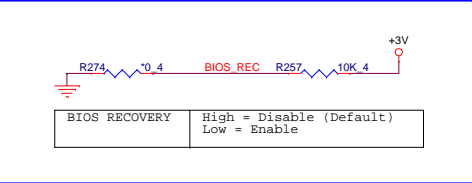
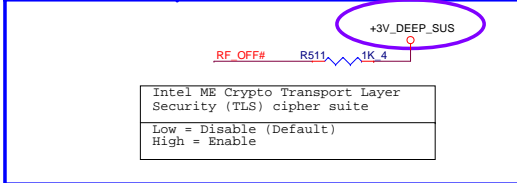
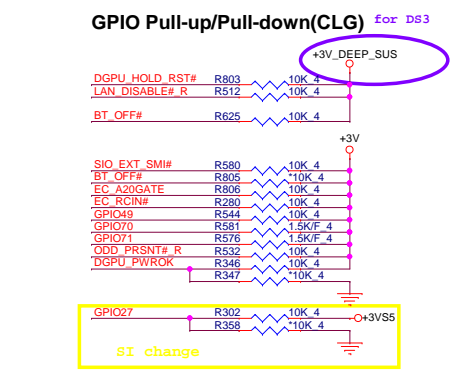
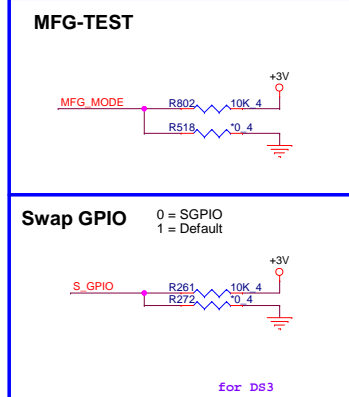
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx



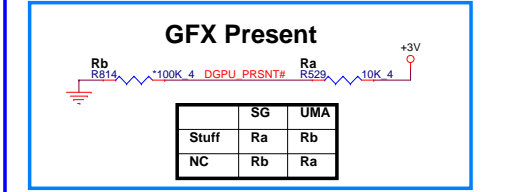
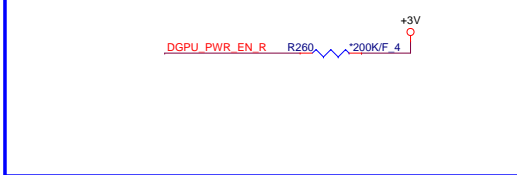
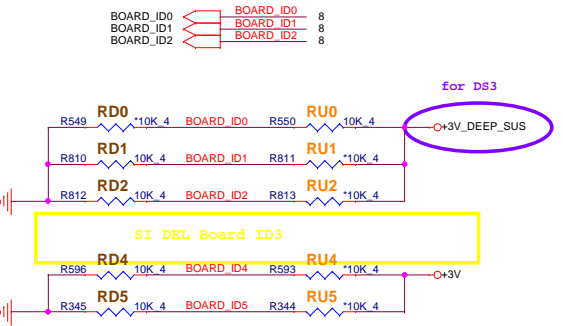
SI add



BOARD ID SETTING

BOARD_ID1 For Stage Use

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R62 UMA			0	0	0	0
DB R62 DIS			0	0	1	1
			0	1	1	1
			1	1	1	1
			0	0	0	0



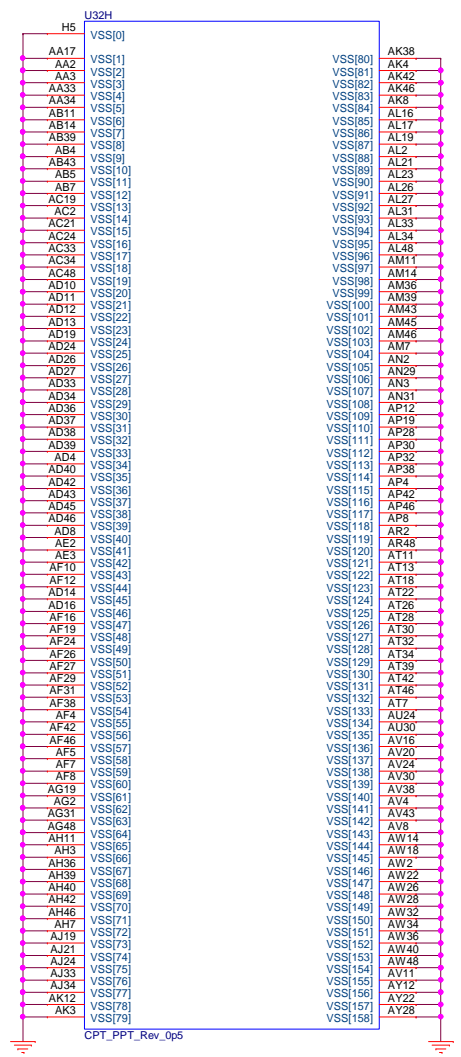
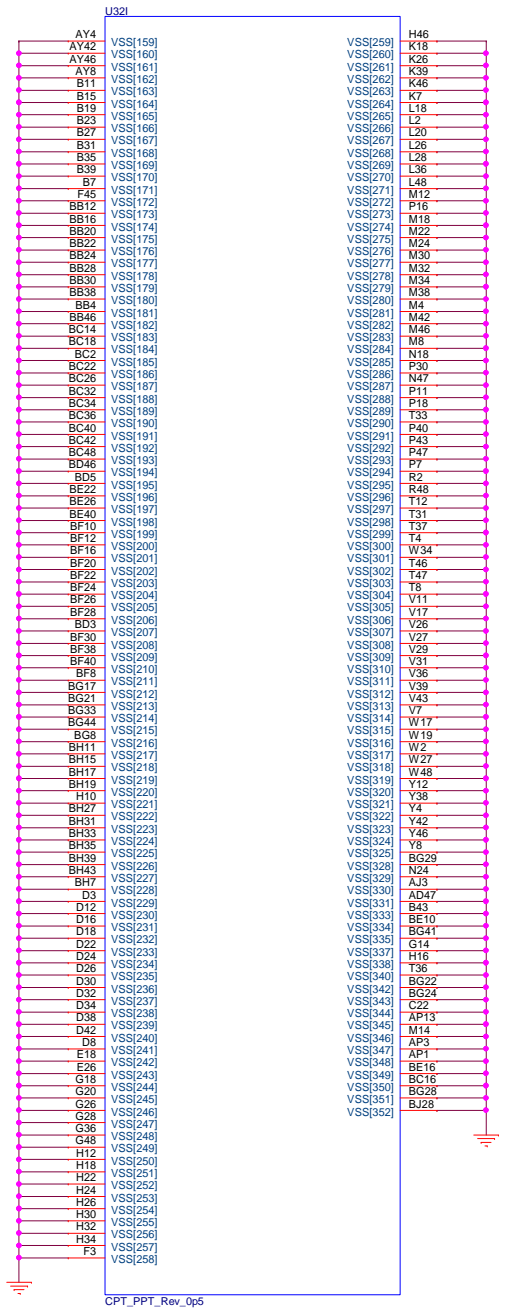
PROJECT : R62
Quanta Computer Inc.

NB5

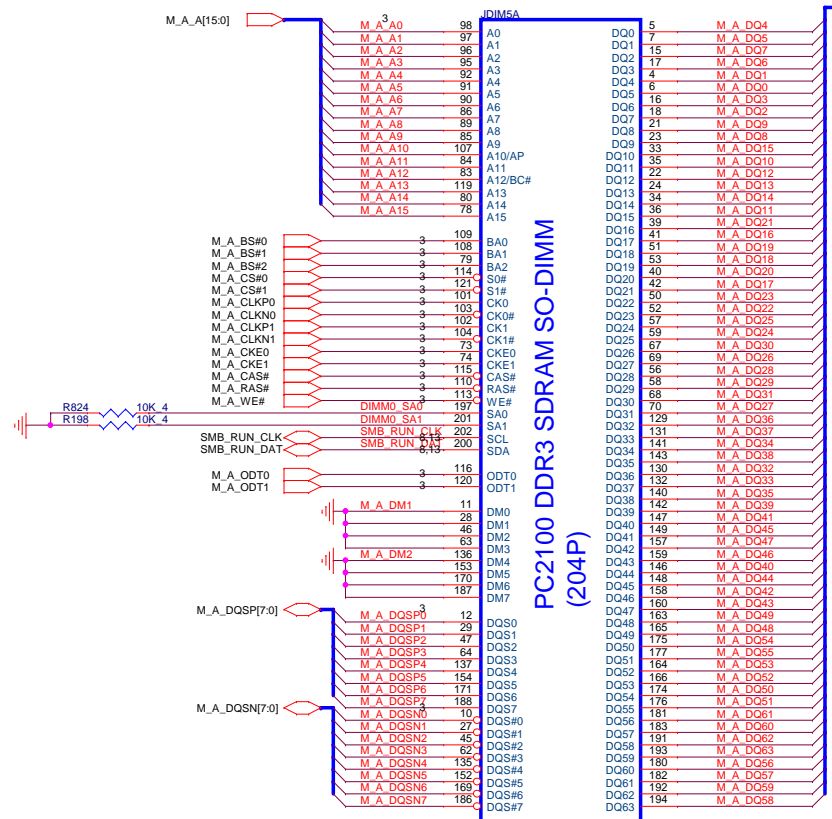
Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
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Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)

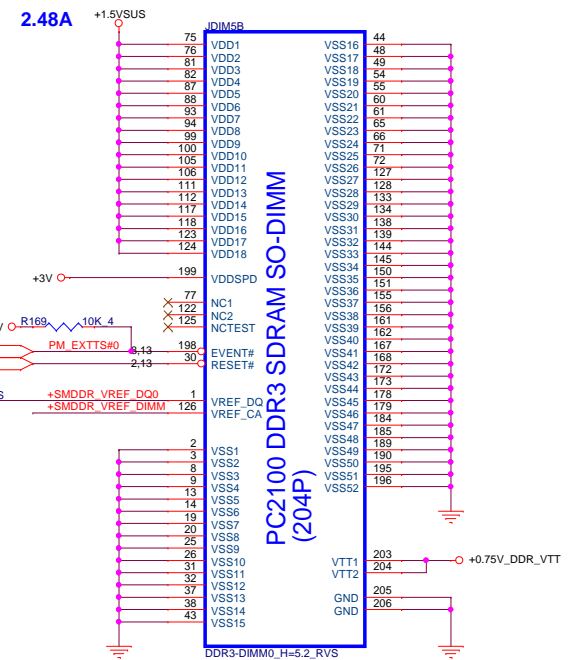
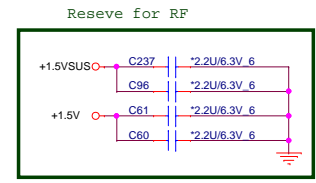


	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (GND)	
Date: Monday, October 22, 2012		Sheet 11 of 43	



PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=5.2_RVS
 ddr-78279-001-rvs-204p
 DGMK4000278
 SOCKET DDR3 SODIMM(204P,H5.2,RVS)QBCON

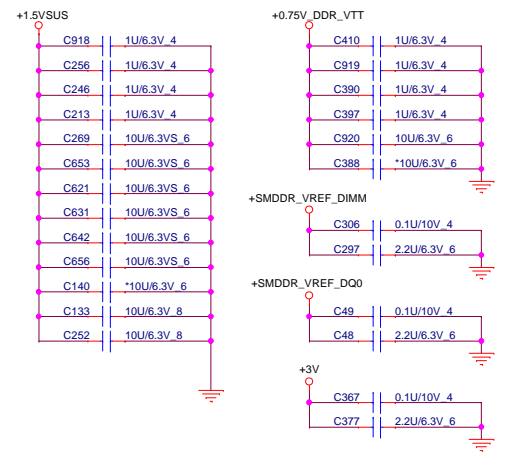


PC2100 DDR3 SDRAM SO-DIMM (204P)

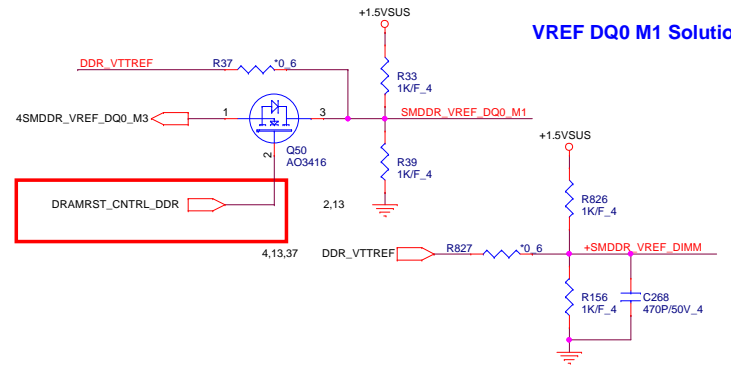
DDR3-DIMM0_H=5.2_RVS
 ddr-78279-001-rvs-204p
 DGMK4000278
 SOCKET DDR3 SODIMM(204P,H5.2,RVS)QBCON

- +1.5V 4,10,27,33
- +0.75V_DDR_VTT 3,37,39
- +1.5VSUS 2,4,13,37,43
- +3VPCU 5,7,25,30,31,33,34,35
- +3V 2,6,7,8,9,10,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42

Place these Caps near So-Dimm0.



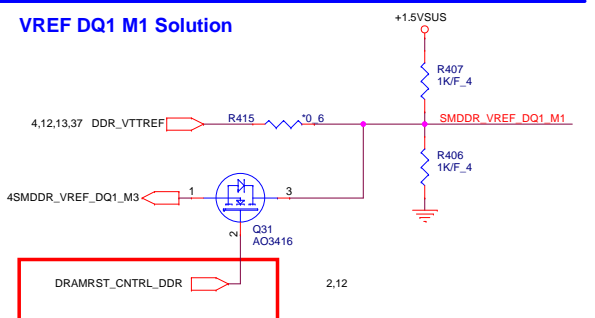
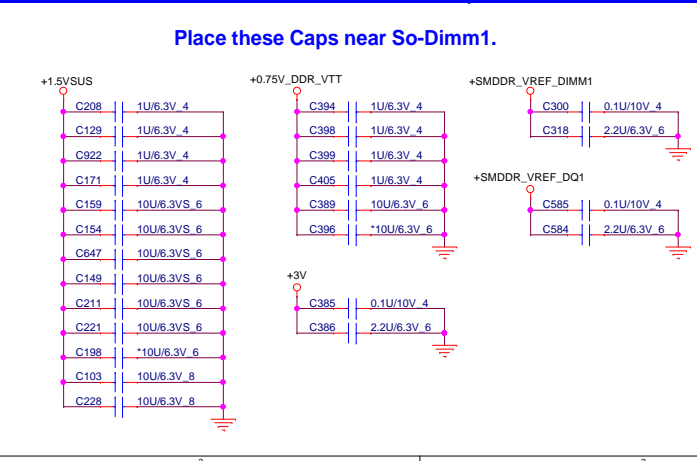
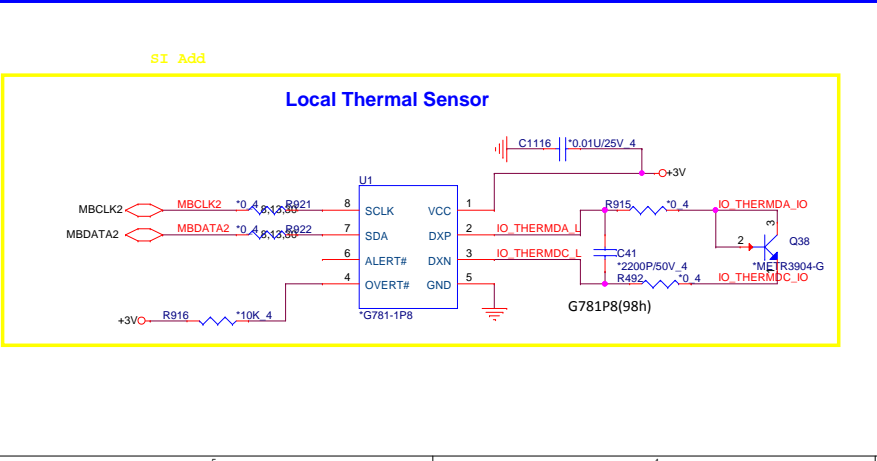
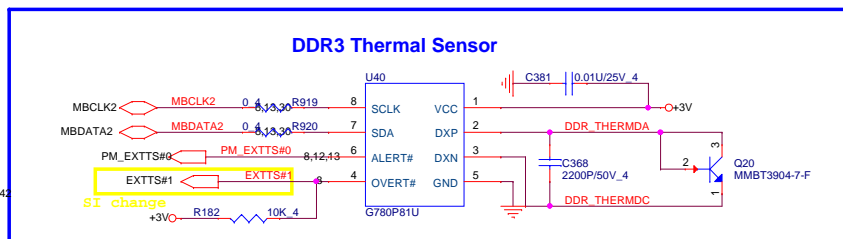
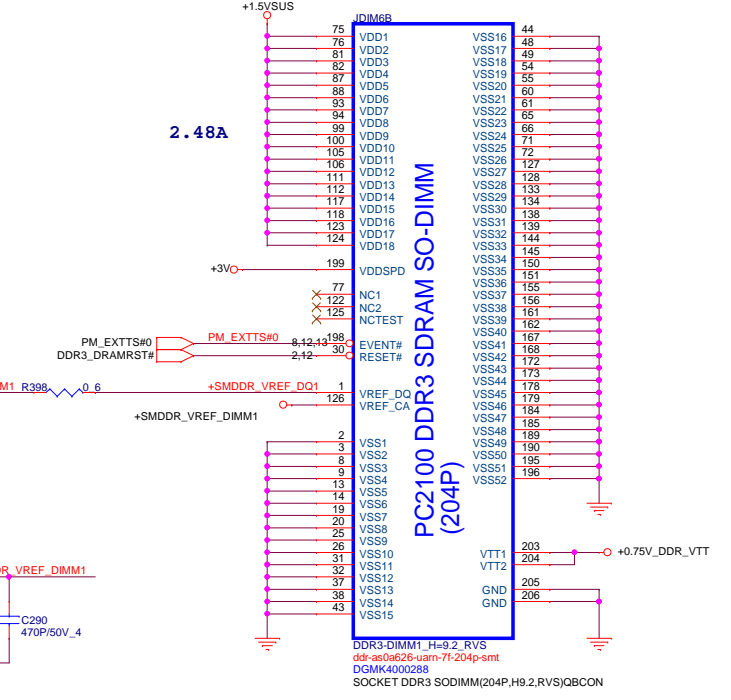
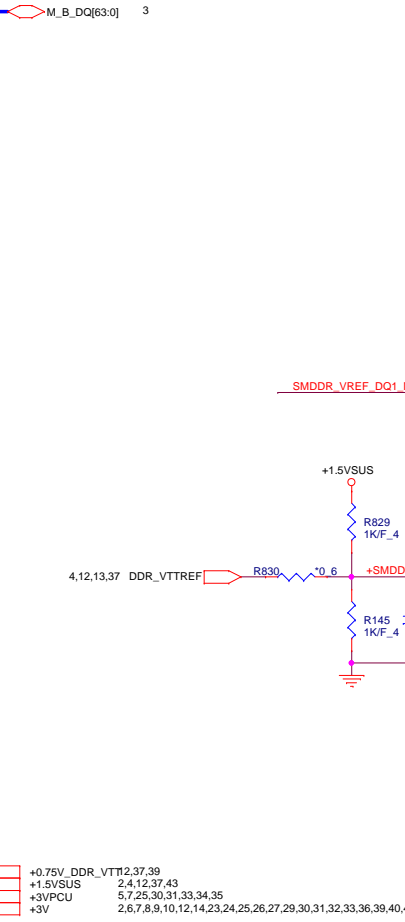
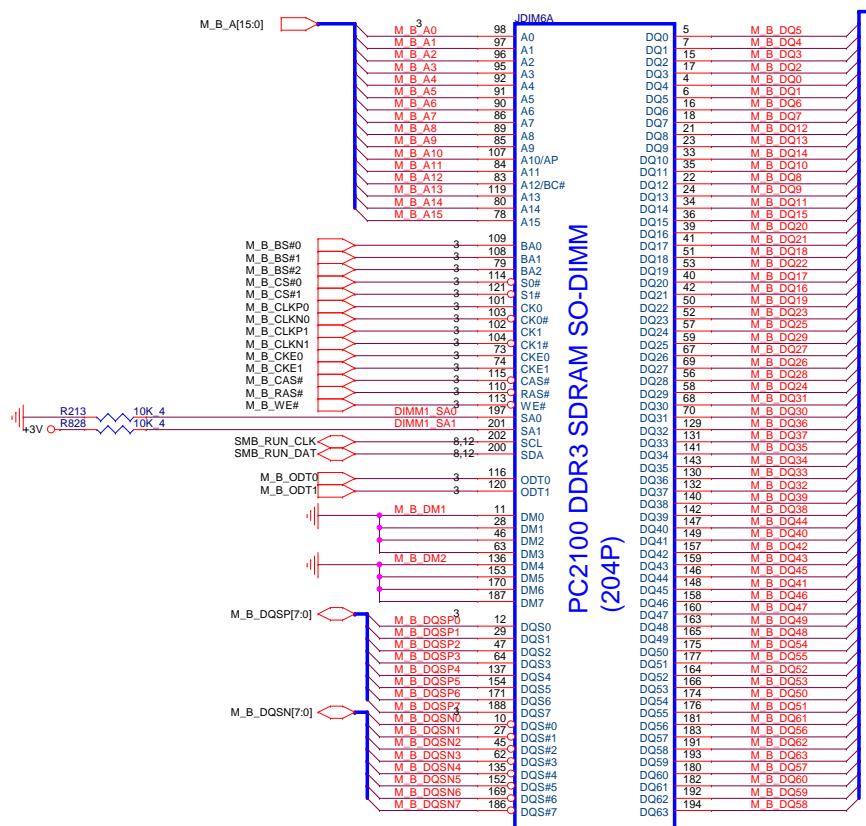
VREF DQ0 M1 Solution



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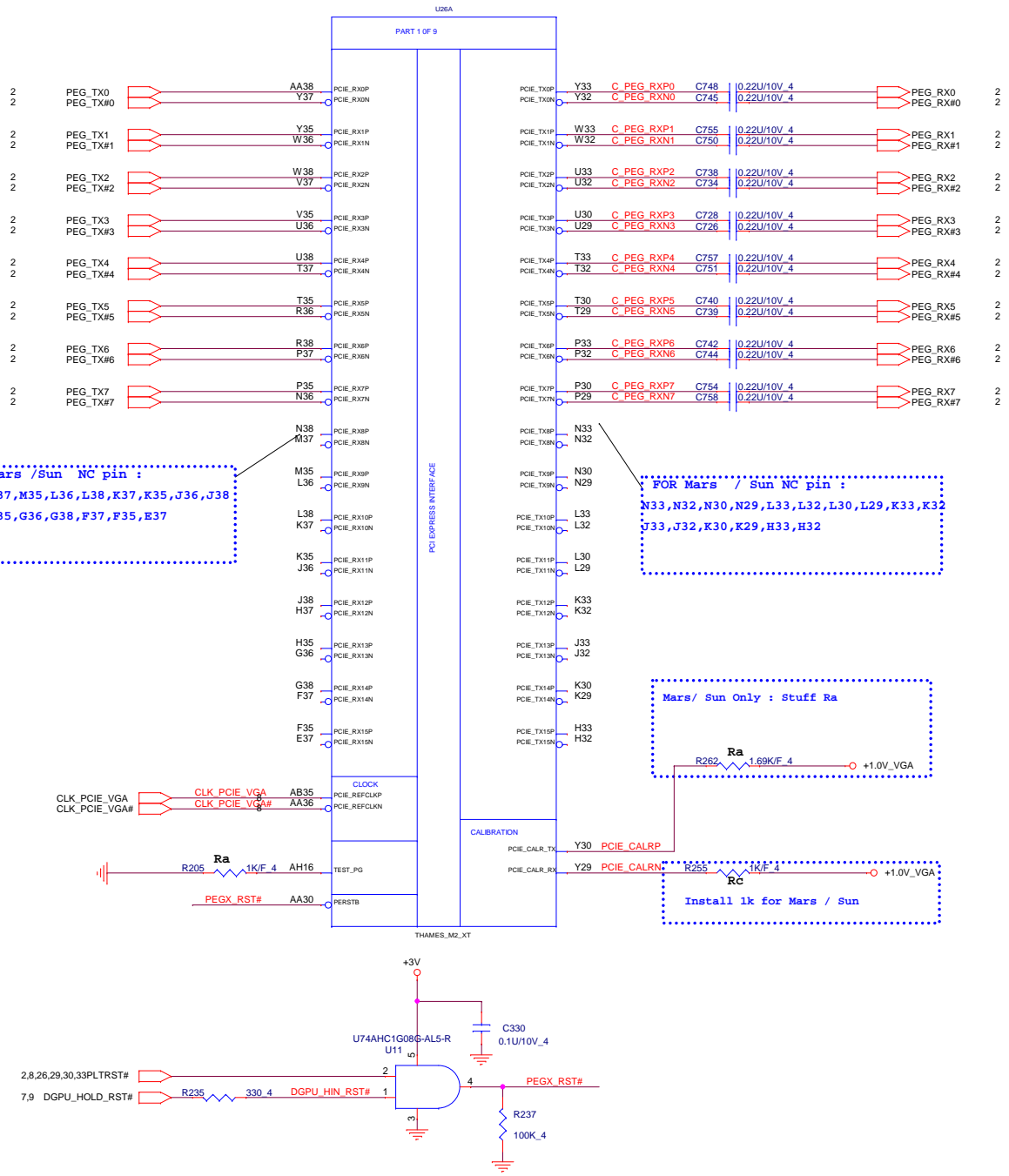
NBS

Size Custom	Document Number DDR3 DIMM0-RVS (5.2H)	Rev 1A
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NB5	Size	Document Number	Rev
	Custom	DDR3 DIMM1-RVS (9.2H)	1A
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For Mars /Sun NC pin :
 N38, M37, M35, L36, L38, K37, K35, J36, J38,
 H37, H35, G36, G38, F37, F35, E37

FOR Mars / Sun NC pin :
 N33, N32, N30, N29, L33, L32, L30, L29, K33, K32,
 J33, J32, K30, K29, H33, H32

Mars/ Sun Only : Stuff Ra

Install 1k for Mars / Sun

2,6,7,8,9,10,14,21,23,24,25,26,27,29,30,31,32,33,36,39,40,42
 16,18,19,43 +1.0V_VGA

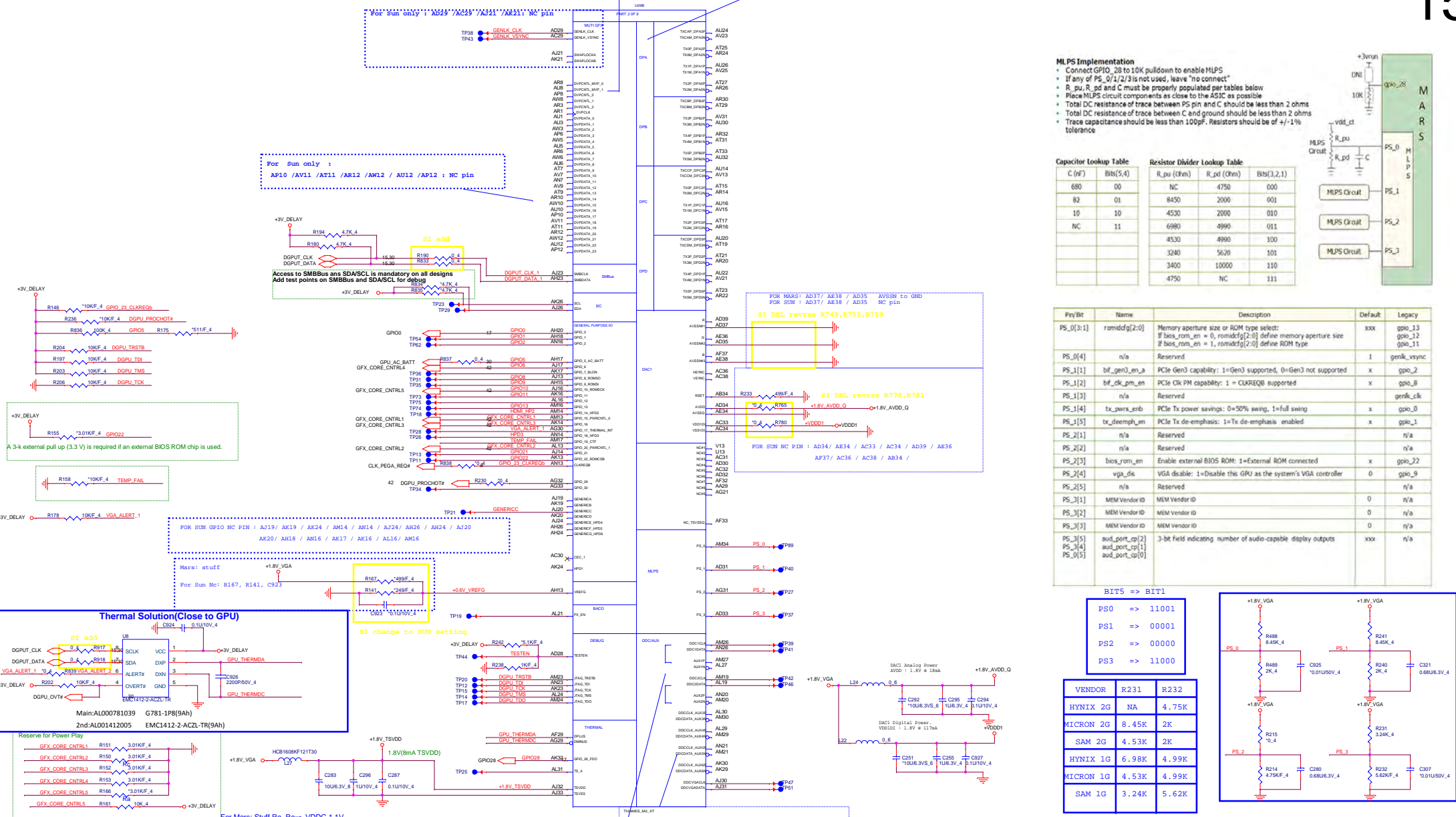
	PROJECT : R62 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number THAMES_PCIE_Interface	
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For Mars / Sun : AR3/AR6/AR3/AR8/AU8: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only : AP10 / AV11 / AT11 / AR12 / AM12 / AU12 / AP12 : NC pin

Access to SMBus and SDA/SCL is mandatory on all designs. Add test points on SMBus and SDA/SCL for debug.



MLPS Implementation

- Connect GPIO_28 to 10K pull-down to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between P and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/- 1% tolerance

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bits	Name	Description	Default	Legacy
PS_0[3:1]	romidg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidg[2:0] define memory aperture size. If bios_rom_en = 1, romidg[2:0] define ROM type	xxx	gpio_13, gpio_12, gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQ supported	x	gpio_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwr_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[5]	vga_ds	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_ep[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[6]	aud_port_ep[1]			
PS_3[5]	aud_port_ep[0]			

BIT5 => BIT1

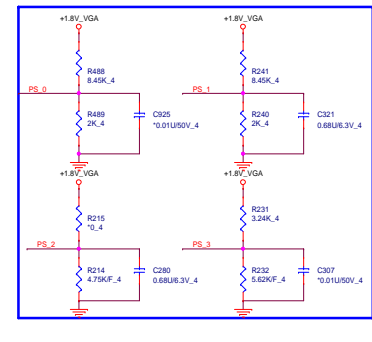
PS0 => 11001

PS1 => 00001

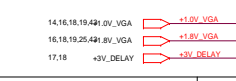
PS2 => 00000

PS3 => 11000

VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K

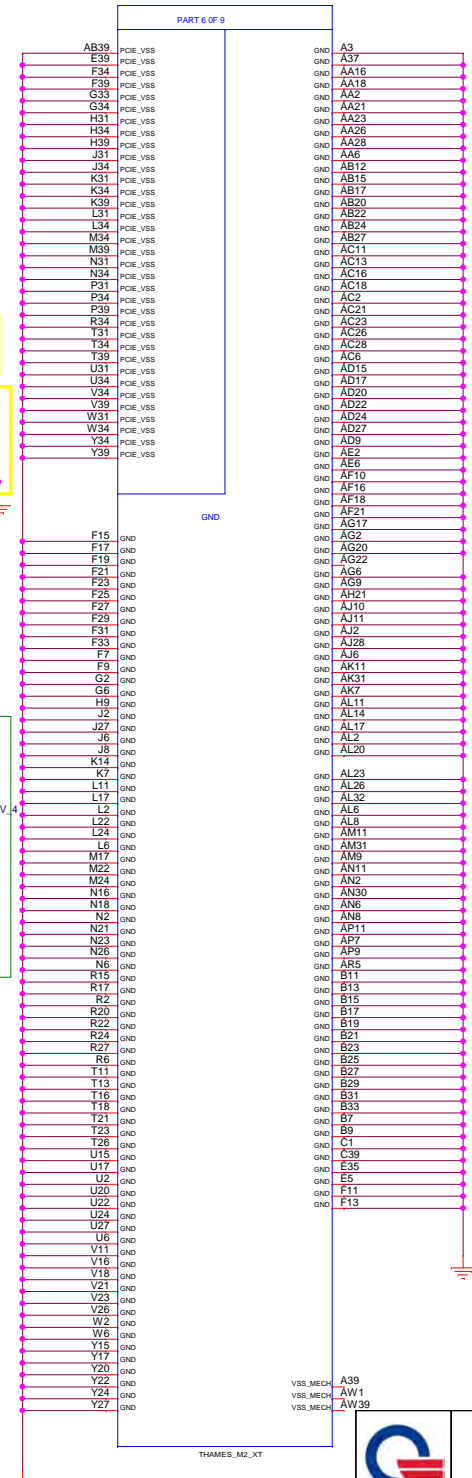
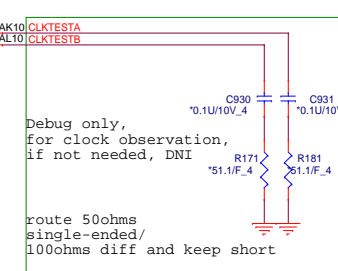
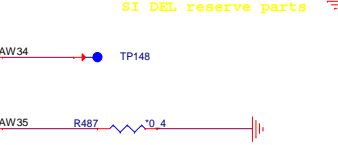
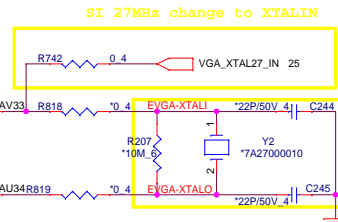
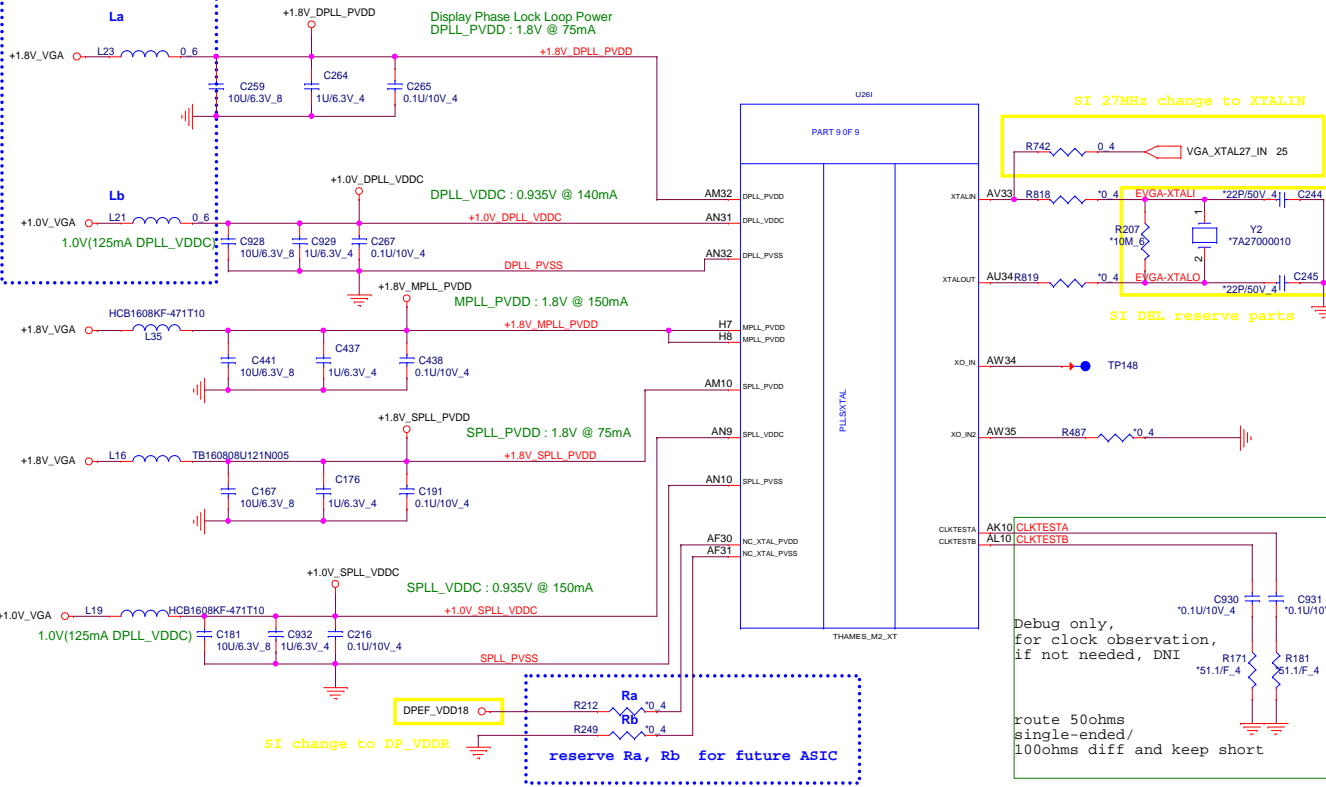


PS3 BIT5=>BIT1	ID	Memory Type	Configuration	Pin	Channel Size	
000	0	Hynix	H5TC4G63AFR-11C	250Mx16 *4 pcs	AKD5PW2TW08 IC SDRAM/6P/H5TC4G63AFR-11C	2G
001	1	Micron	MT41J255M16HA-093GE	250Mx16 *4 pcs	AKD5PZ3T1L01 IC SDRAM/6P/MT41J255M16HA-093GE	2G
010	2	Samsung	K4W4G1646B-HC1A	250Mx16 *4 pcs	AKD5PZD1501 IC SDRAM/6P/K4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FR-11C	128Mx16 *4 pcs	AKD5MZD1W03 IC SDRAM/6P/H5TC2G63FR-11C	1G
100	4	Micron	MT41L128M16JT-093CE	128Mx16 *4 pcs	AKD5MZD1W03 IC SDRAM/6P/MT41L128M16JT-093CE	1G
101	5	Samsung	K4W2G1646E-BC1A	128Mx16 *4 pcs	AKD5MGT535 IC SDRAM/6P/K4W2G1646E-BC1A	1G

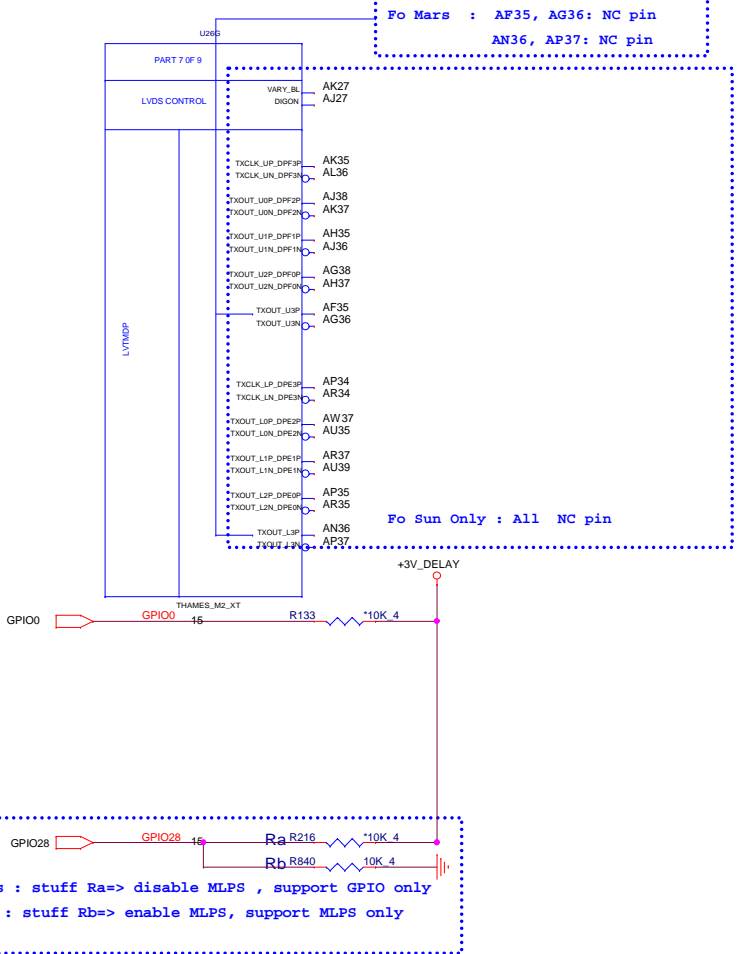


Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm



PROJECT : R62
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Thems : stuff Ra=> disable MLPS , support GPIO only
 Mars : stuff Rb=> enable MLPS, support MLPS only

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

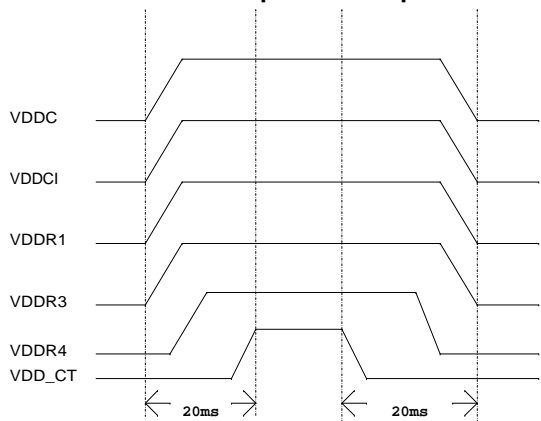
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P05A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9	BIOSROM	GPIO13	ROMIDCFG2	GPIO12	ROMIDCFG1	GPIO11	ROMIDCFG0
0	128M	0	0	0	0	0	0
0	256M	0	0	0	0	1	0
0	64M	0	0	1	0	0	0
0	32M	0	0	1	1	0	0
0	512M	1	1	0	0	0	0
0	1G	1	1	0	0	1	0
0	2G	1	1	1	0	0	0
0	4G	1	1	1	1	0	0

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

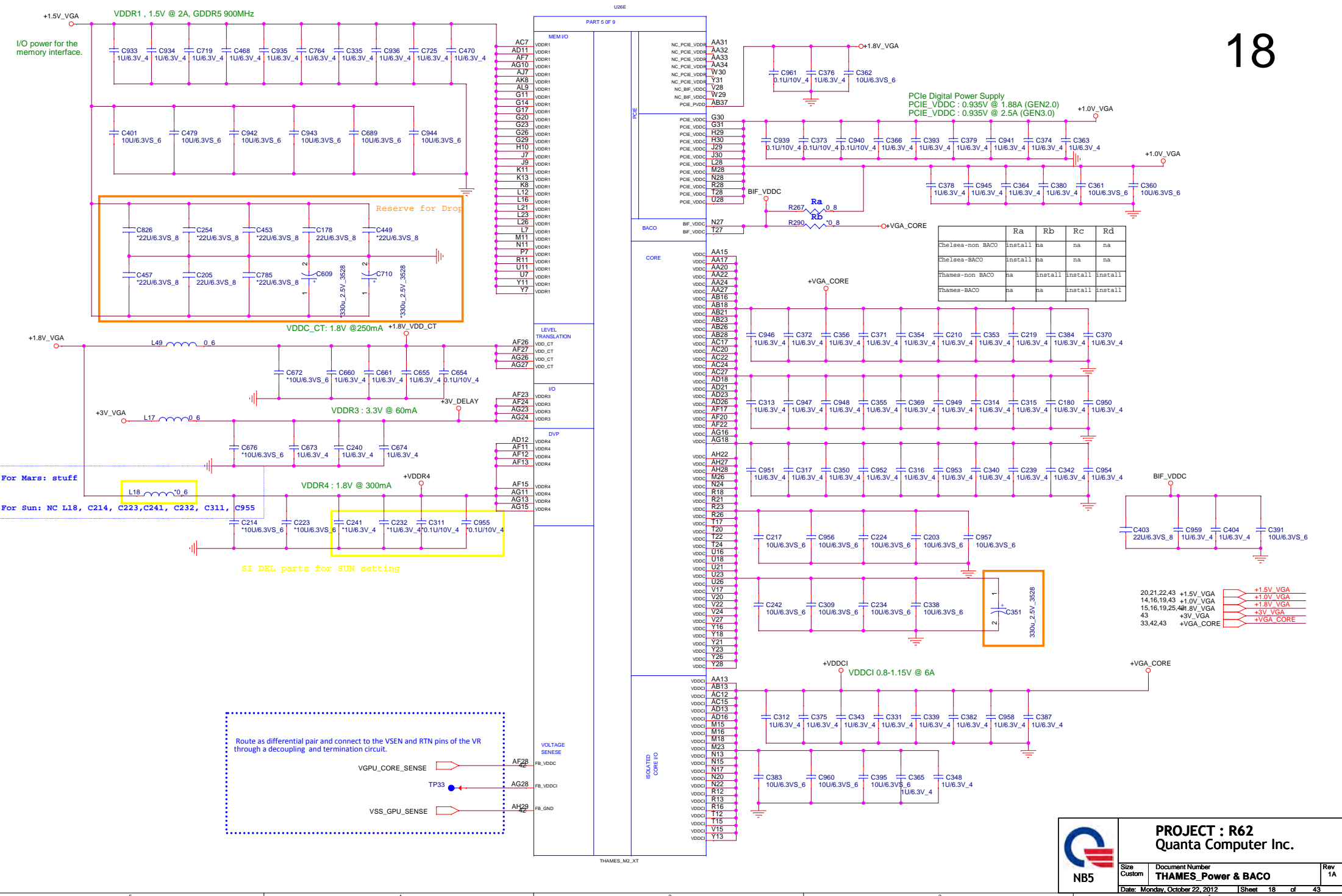
Power Up/Down Sequence



PROJECT : R62
 Quanta Computer Inc.

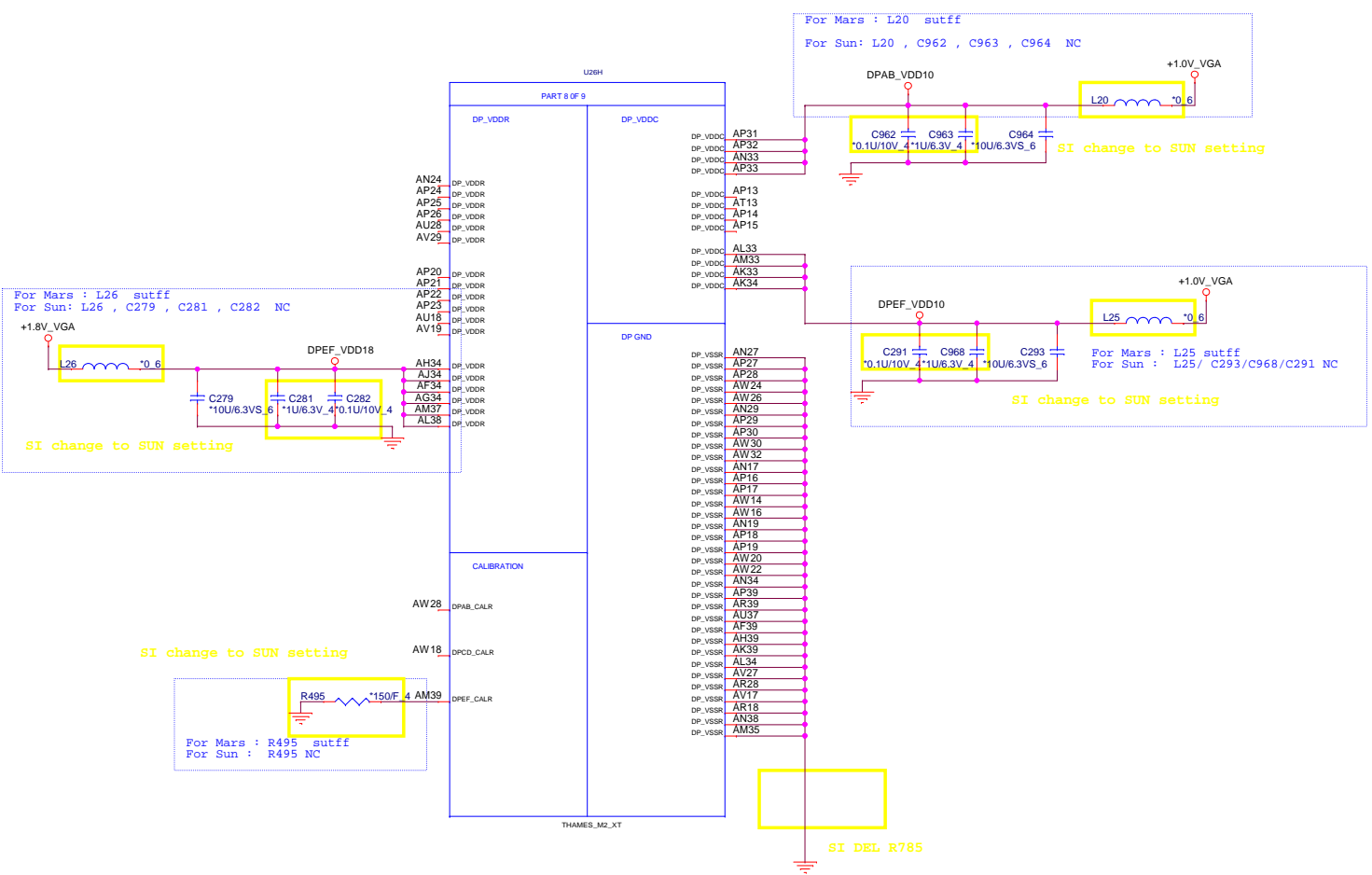
NB5

Size Custom Document Number THAMES_LVDS / STRAP Rev 1A
 Date: Monday, October 22, 2012 Sheet 17 of 43



PROJECT : R62
Quanta Computer Inc.

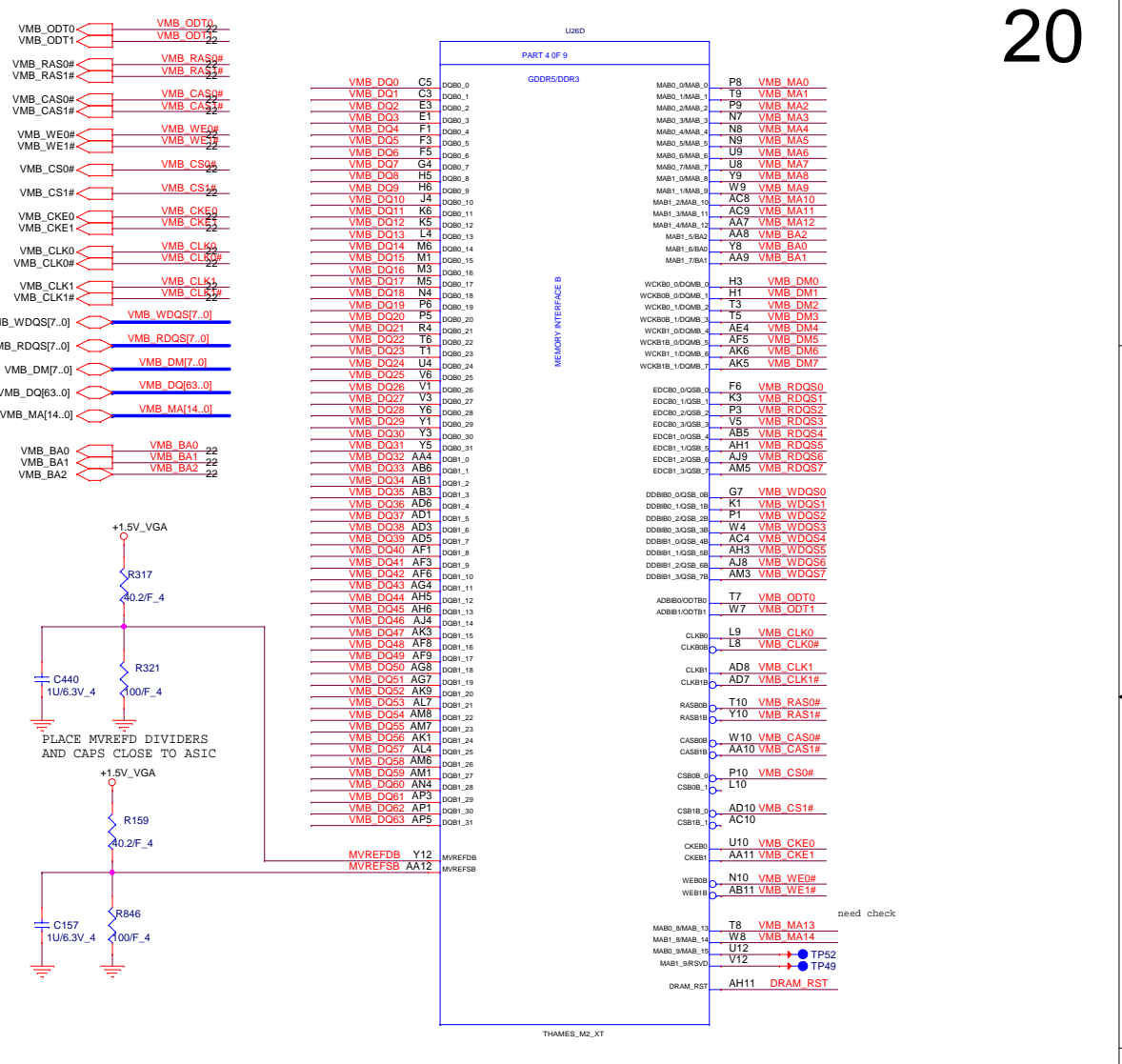
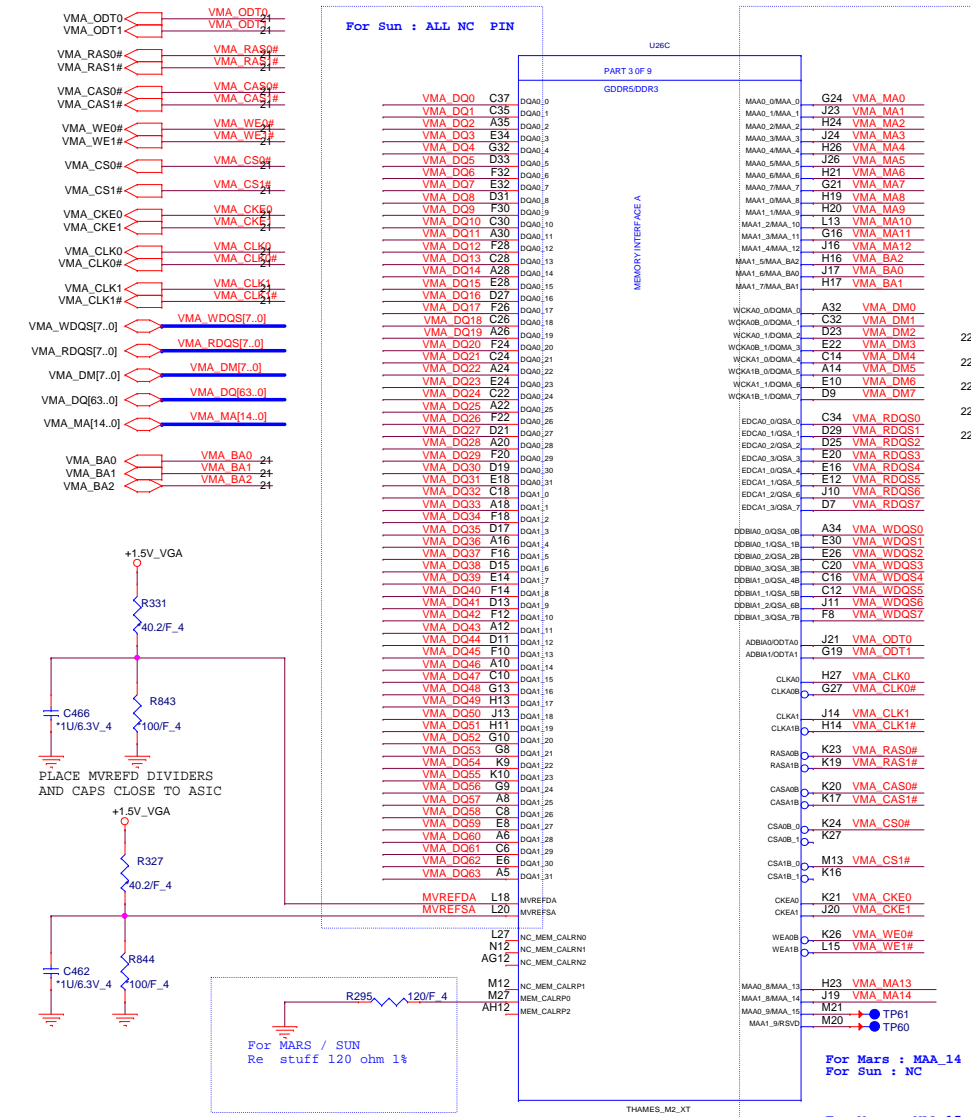
Size Custom	Document Number THAMES_Power & BACO	Rev 1A
Date: Monday, October 22, 2012 Sheet 18 of 43		



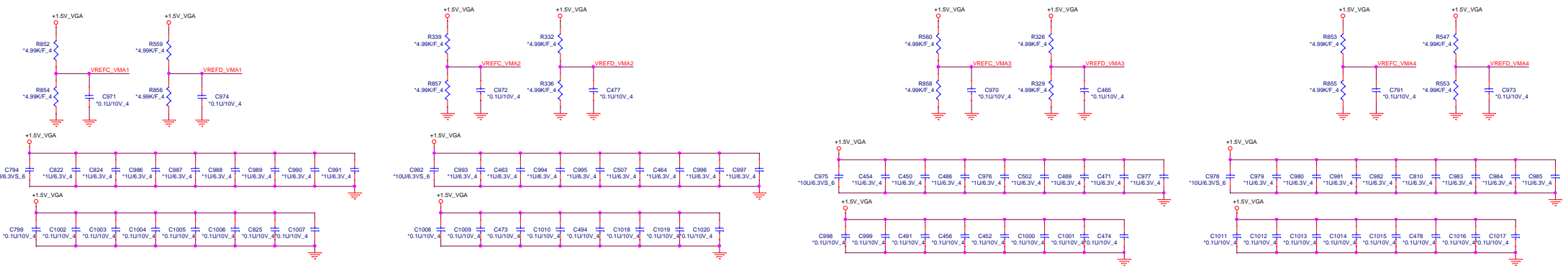
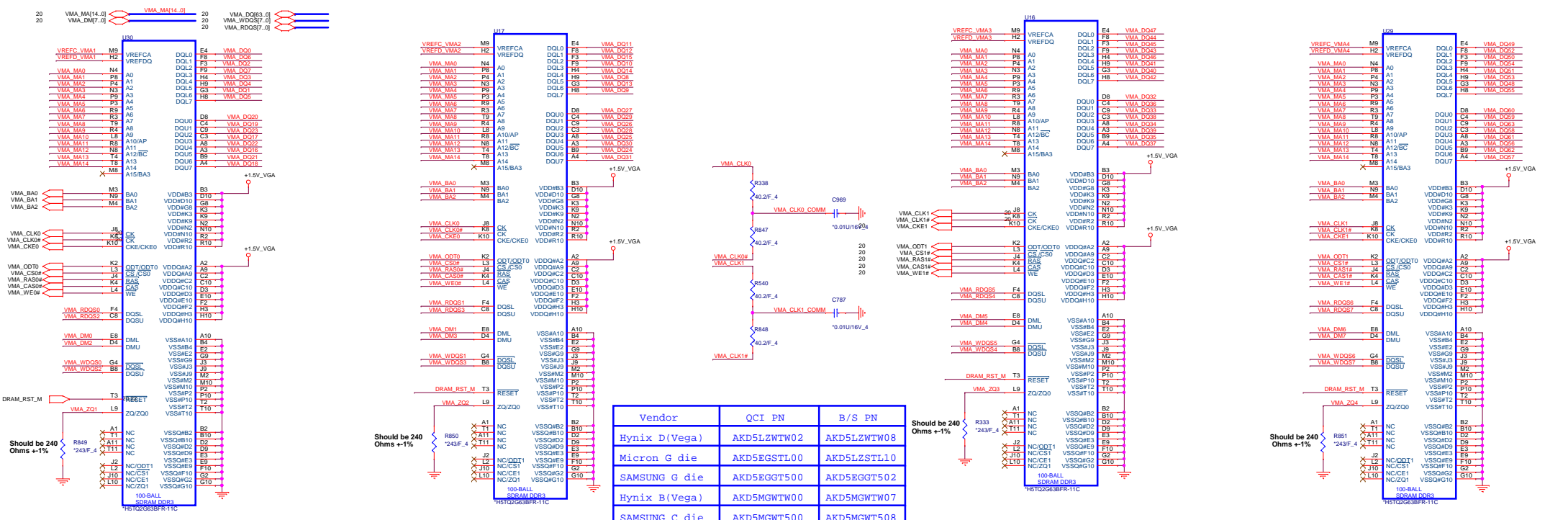
14,16,18,43 +1.0V_VGA
15,16,18,25,40,1.8V_VGA

+1.0V_VGA
+1.8V_VGA

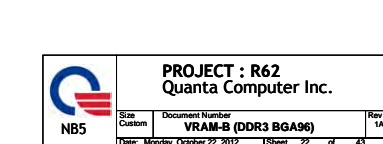
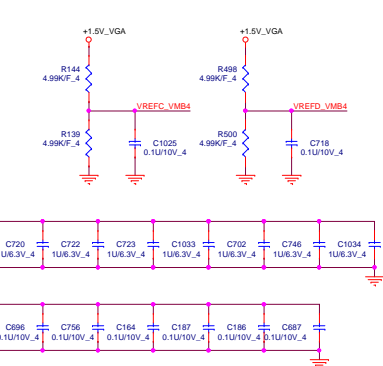
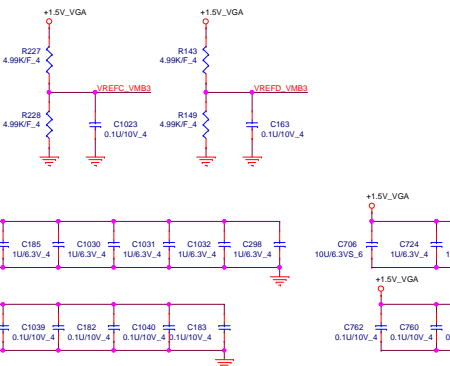
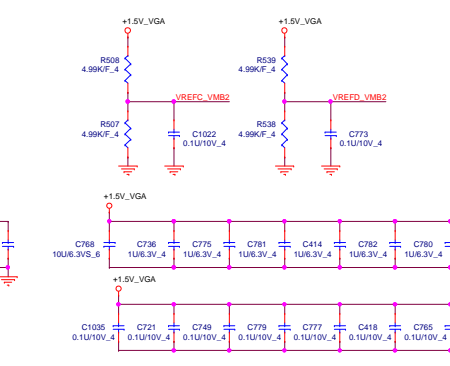
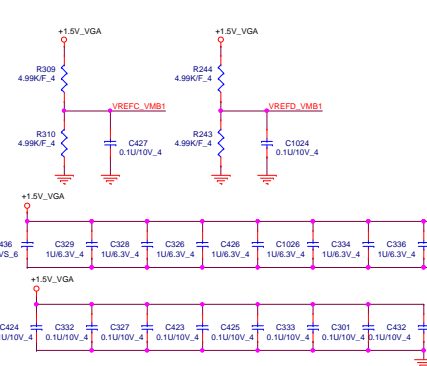
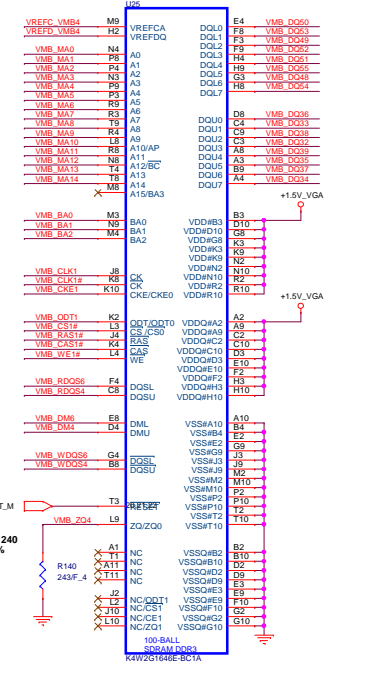
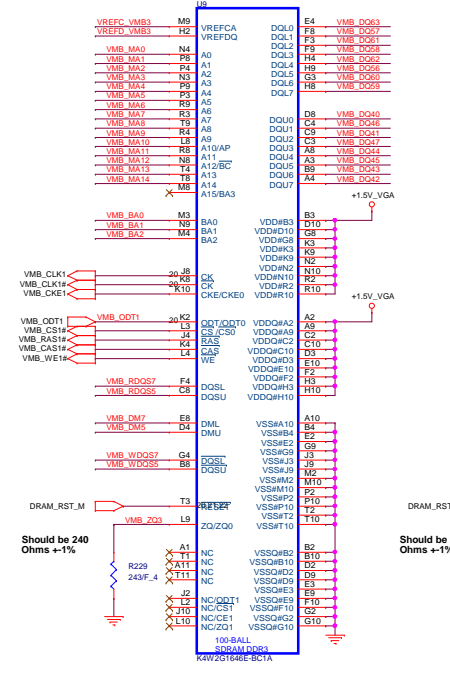
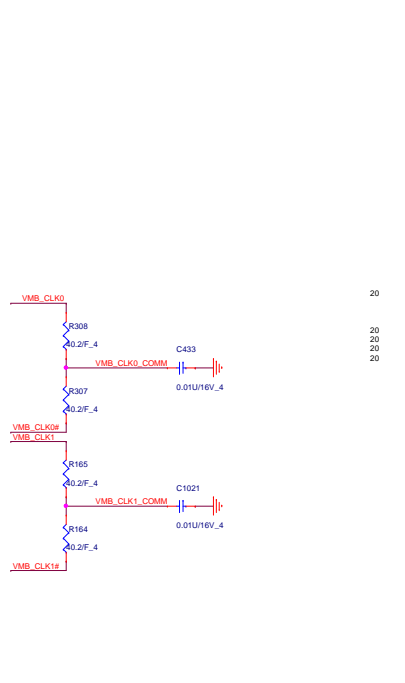
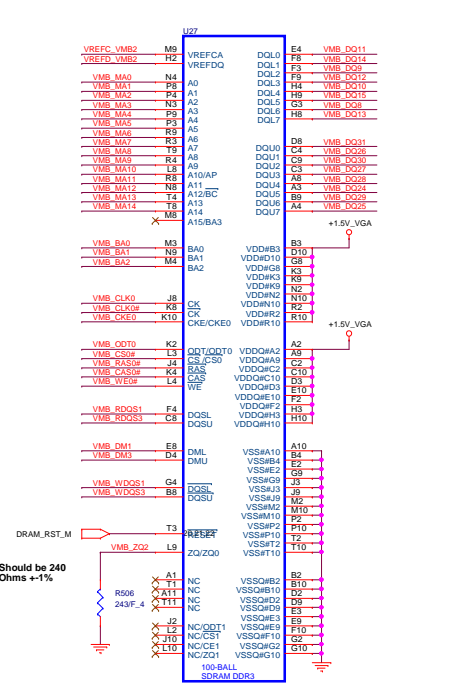
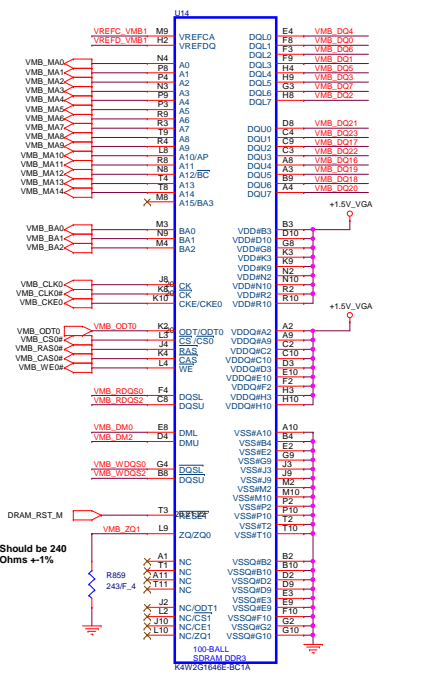
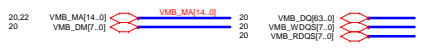
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number THAMES_DP Powers	
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CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3



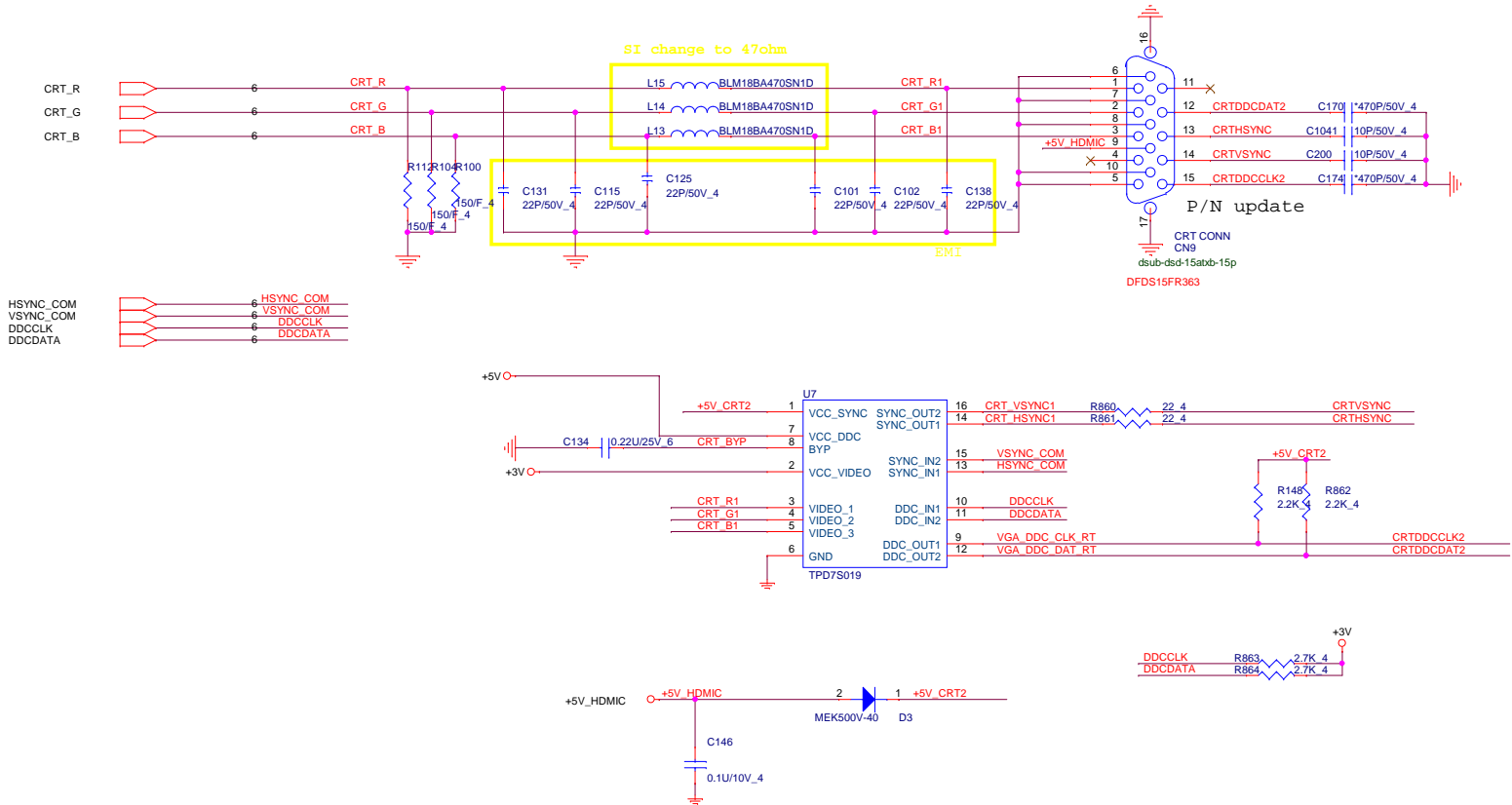


PROJECT : R62
Quanta Computer Inc.

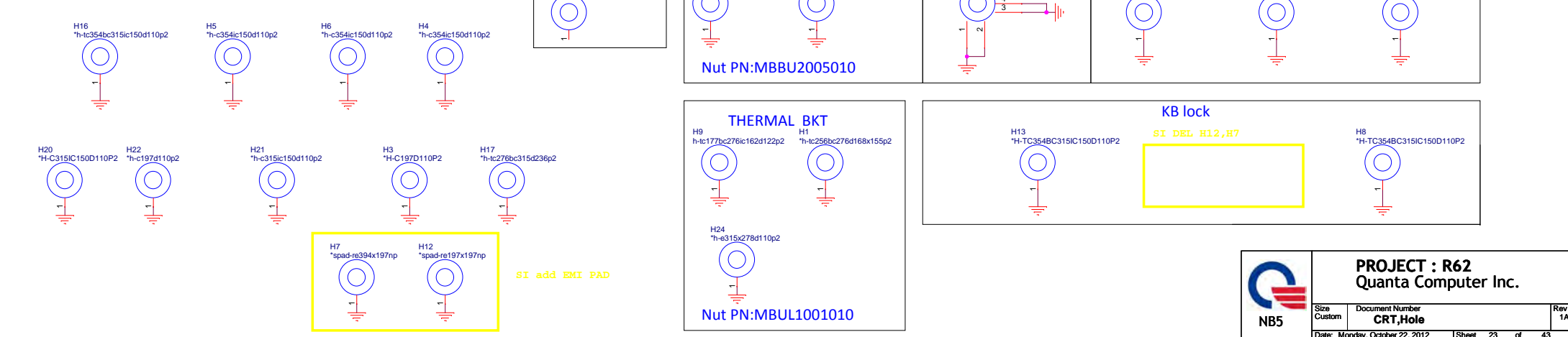
Size	Document Number	Rev
Custom	VRAM-B (DDR3 BGA96)	1A

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7,10,25,27,31,33,33.39
2,6,7,8,9,10,12,15,14,24,25
25
+5V_HDMIC

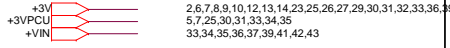
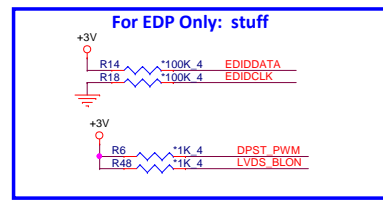
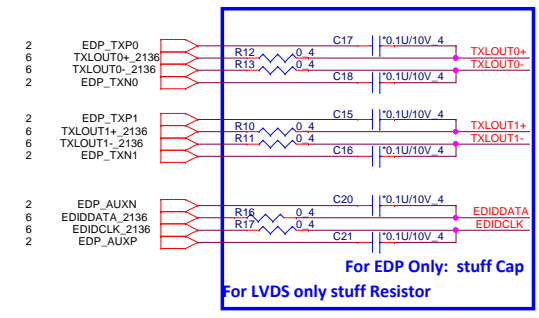
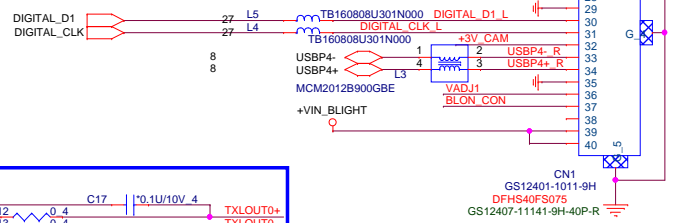
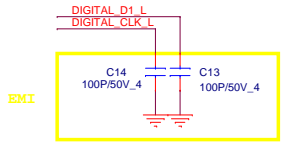
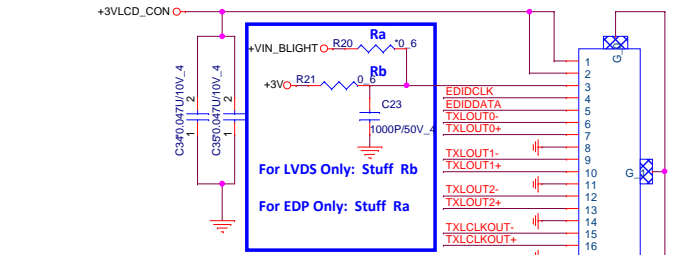
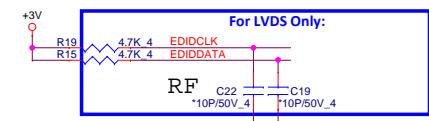
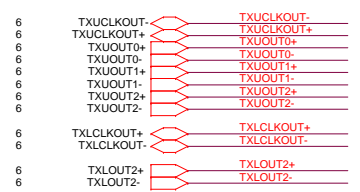
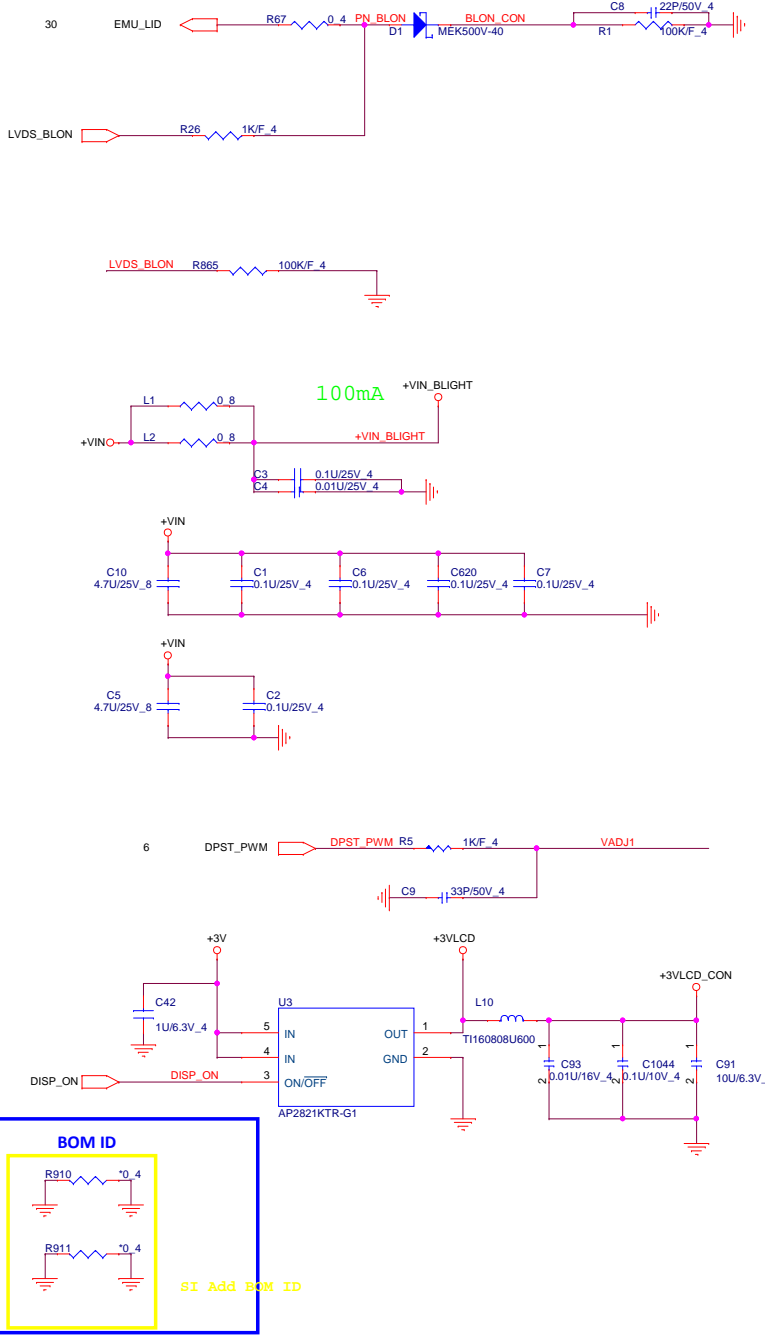


HOLE



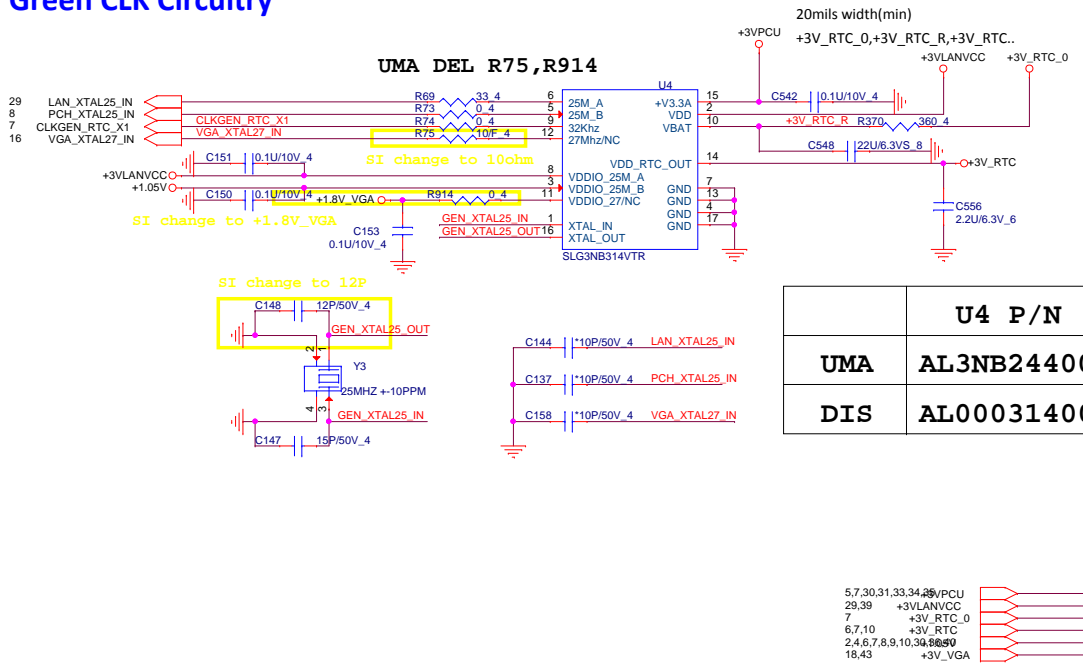
	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number CRT,Hole	Rev 1A
	Date: Monday, October 22, 2012		Sheet 23 of 43

LID Switch

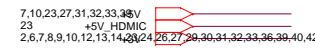
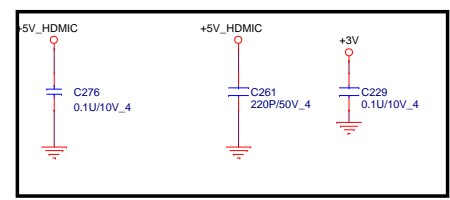


		PROJECT : R62 Quanta Computer Inc.	
		Size Custom Document Number LCD CONN/LID/CAM	Rev 1A
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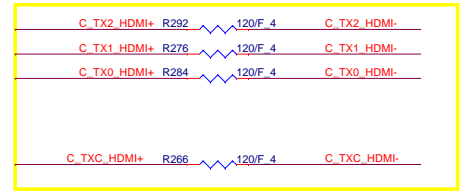
Green CLK Circuitry



EMI request

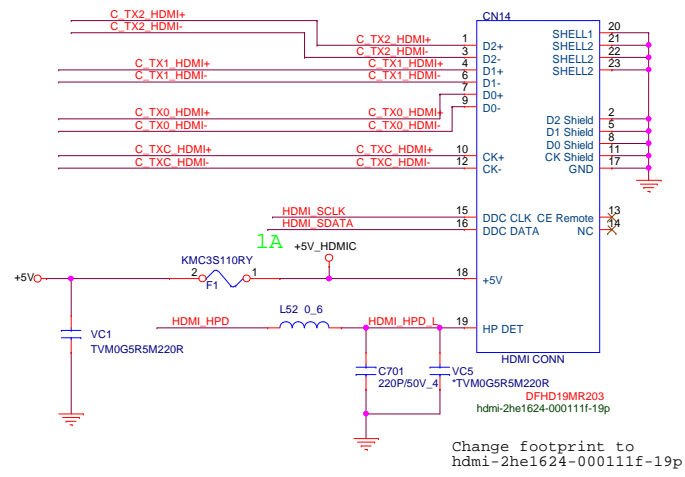
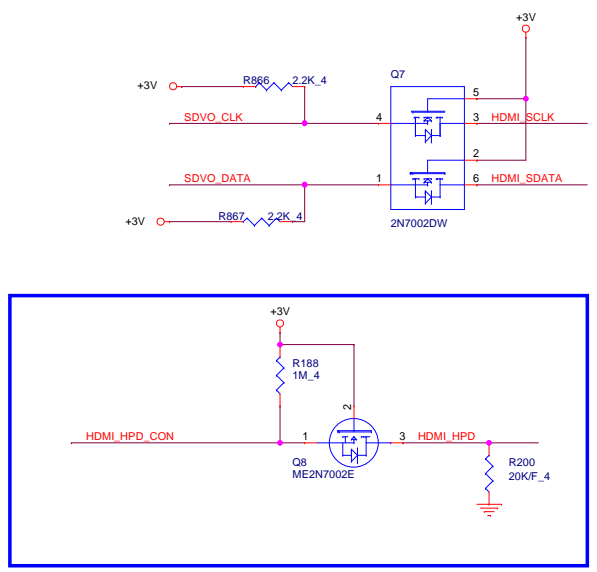
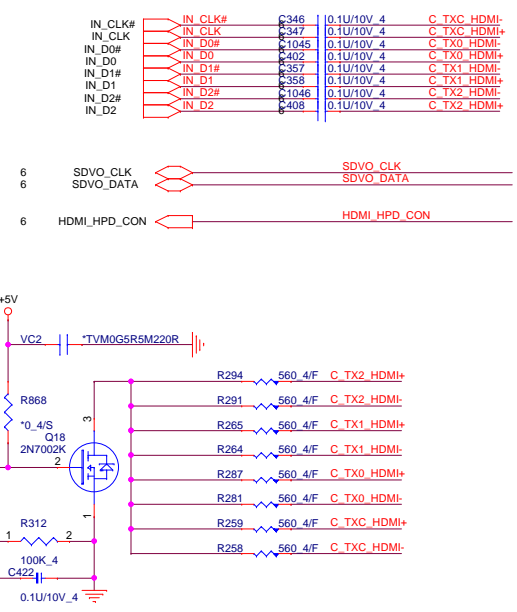


EMI request



close to HDMI conn

Close to HDMI Connector



Change footprint to hdmi-2he1624-000111f-19p

	PROJECT : R62	
	Quanta Computer Inc.	
	Size Custom Document Number HDMI CONN	Rev 1A
Date: Monday, October 22, 2012 Sheet 25 of 43		

8 CLK_PCIE_REQ2# CLK_PCIE_REQ2# R446 0.4S CLK_PCIE_REQ2#_R

SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD_WP	MS_BS

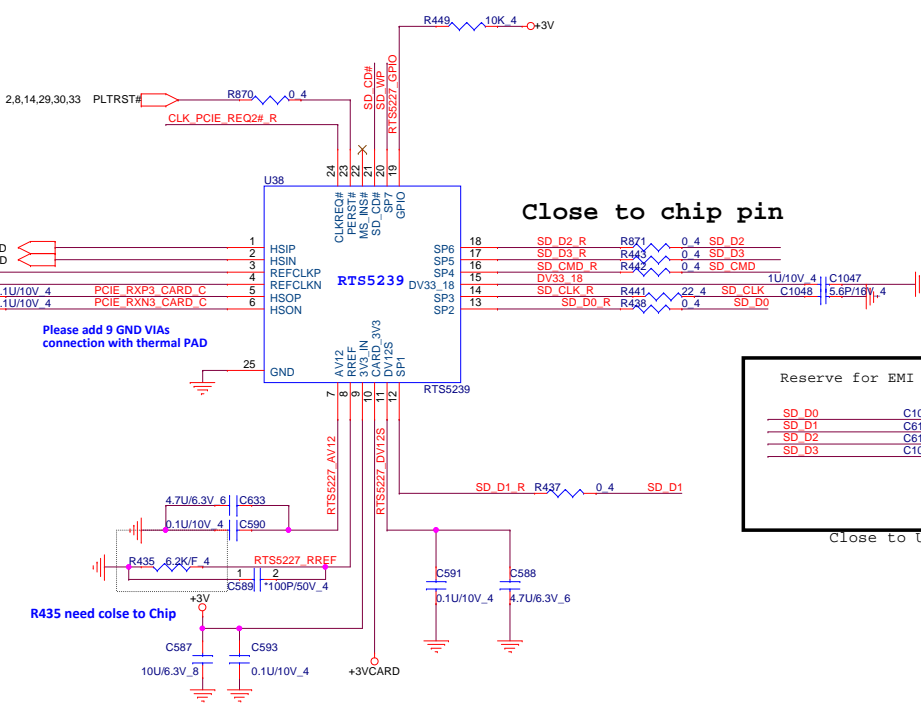
Share Pin

Close to chip pin

Close to chip pin

- 8 CLK_PCIE_CARDP
- 8 CLK_PCIE_CARDN
- 8 PCIE_RXP3_CARD
- 8 PCIE_RXN3_CARD

- 8 PCIE_TXP3_CARD
- 8 PCIE_TXN3_CARD



Please add 9 GND VIAs connection with thermal PAD

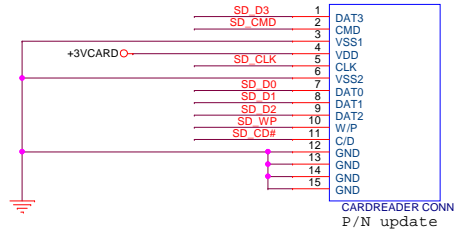
R435 need close to Chip

Reserve for EMI

SD D0	C1069	5.6P/16V_4
SD D1	C612	5.6P/16V_4
SD D2	C611	5.6P/16V_4
SD D3	C1068	5.6P/16V_4

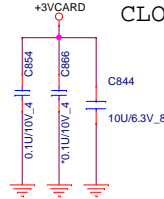
Close to U38

SD / MMC
CARD READER



CARDREADER CONN
P/N update

CLOSE CONN



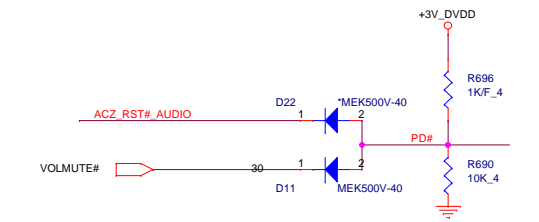
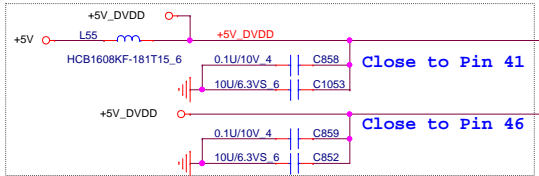
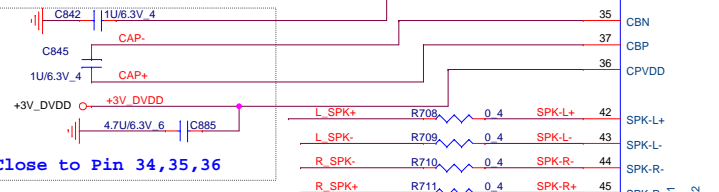
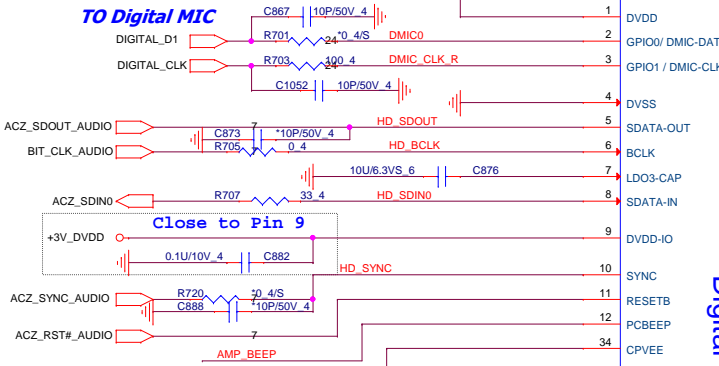
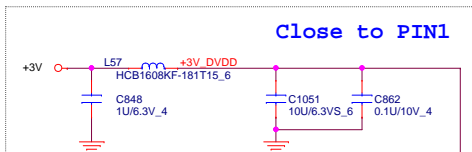
Reserve for EMI

SD D0	C1049	5.6P/16V_4
SD D1	C886	5.6P/16V_4
SD D2	C610	5.6P/16V_4
SD D3	C1050	5.6P/16V_4
SD CLK	C1100	5.6P/16V_4

Close to CN8

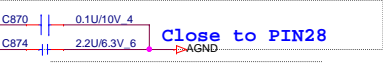
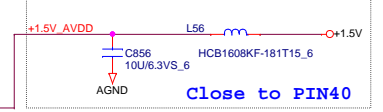
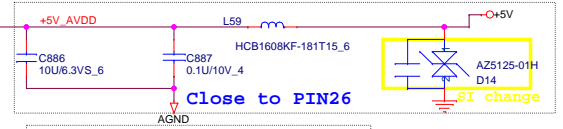
2,6,7,8,9,10,12,13,14,23,24,25,27,29,30,31,32,33,36,39,40,42

	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number RTS5229 & CR SOCKET	
Date: Monday, October 22, 2012		Sheet 26 of 43	



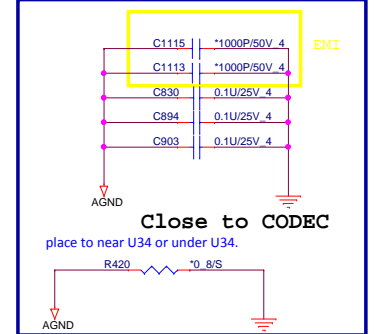
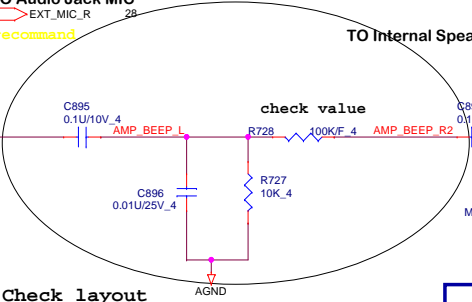
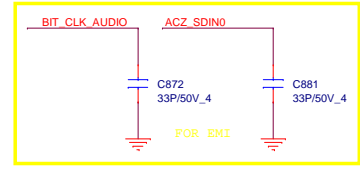
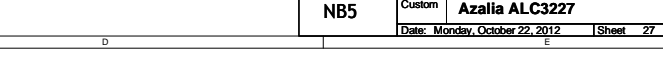
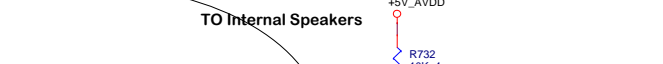
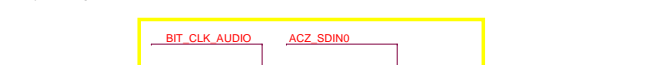
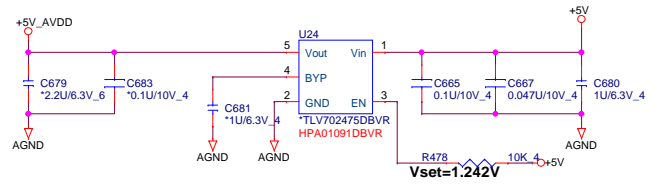
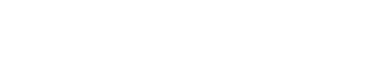
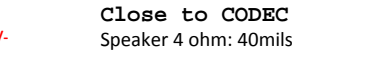
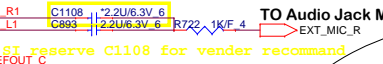
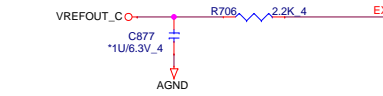
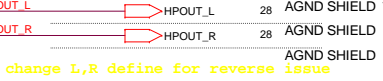
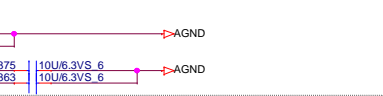
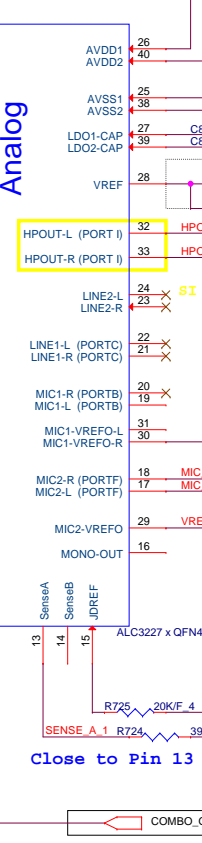
7,10,23,25,31,32,33,39 +5V
2,6,7,8,9,10,12,13,14,23,24,25,29,30,31,32,33,36,39,40,42
4,10,12,33 +1.5V

>40mils trace

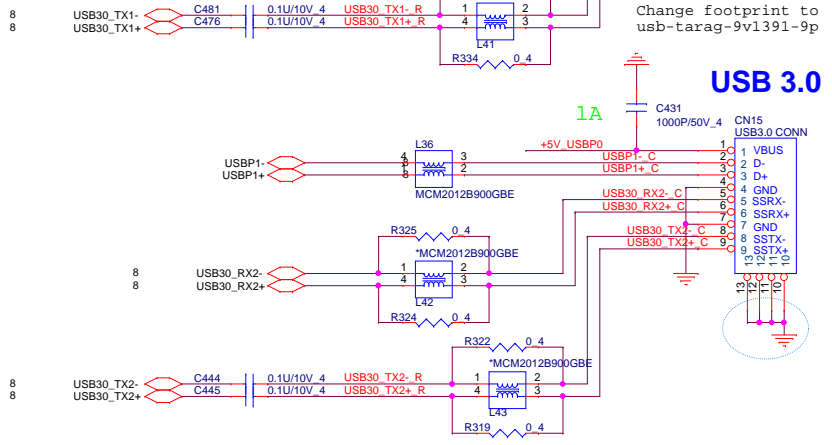
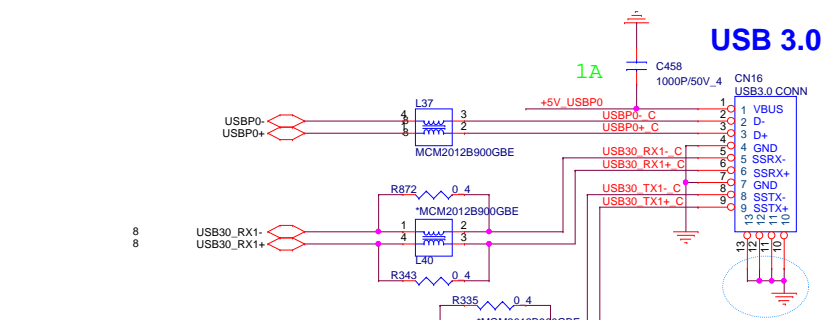
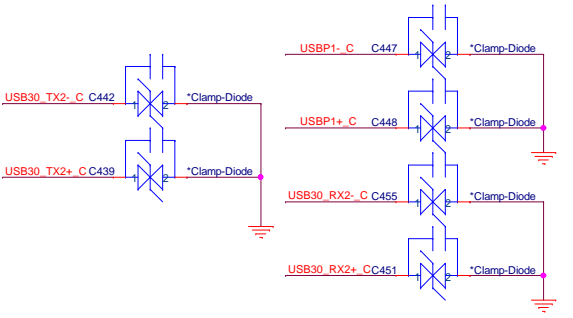
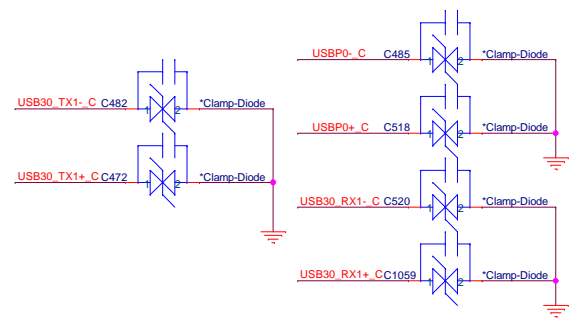


Analog

Digital

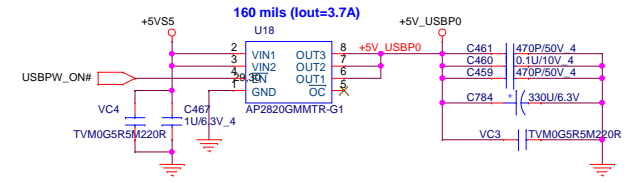


Keep L_SPK+/-, and R_SPK+/- trace width 30 mil least

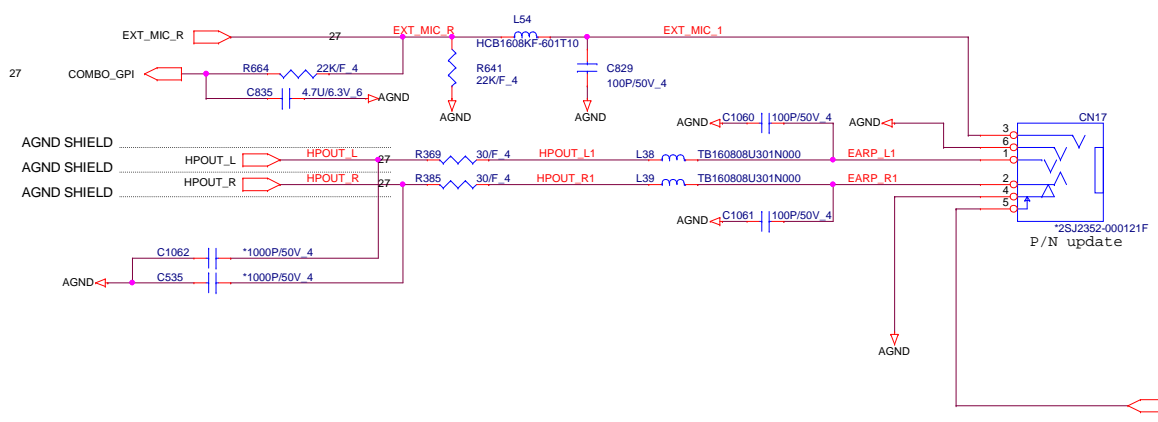


Change footprint to usb-tarag-9v1391-9p

USB3.0 X 2/USB2.0 COMBO

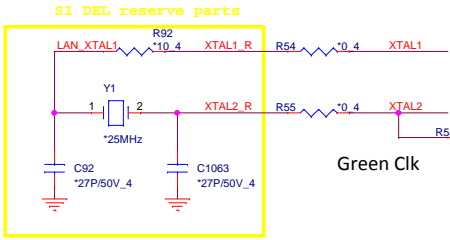


COMBO JACK



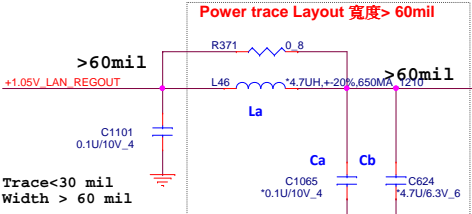
10,29,33,35,36,37,38,39,40,41,42,39
2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
25,29,39 +3VLANVCC

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For GbE
 * Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 22, 8, 30

For 10/100 NA Ce,Cf
 * Place Ce, Cf close to each VDD10 pin-- 8, 30 only,



For GbE
 Stuff La, Ca, Cb

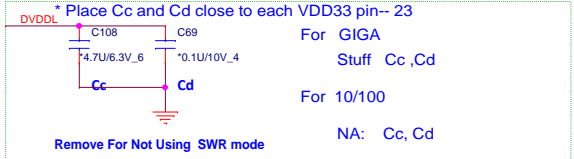
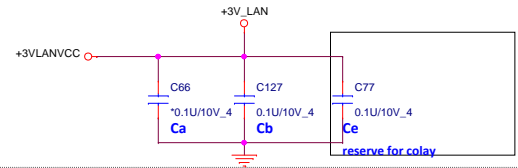
For 10/100
 NA: La, Ca, Cb

For GbE
 * Place Cf close to each VDD10 pin-- 22 (reserve)

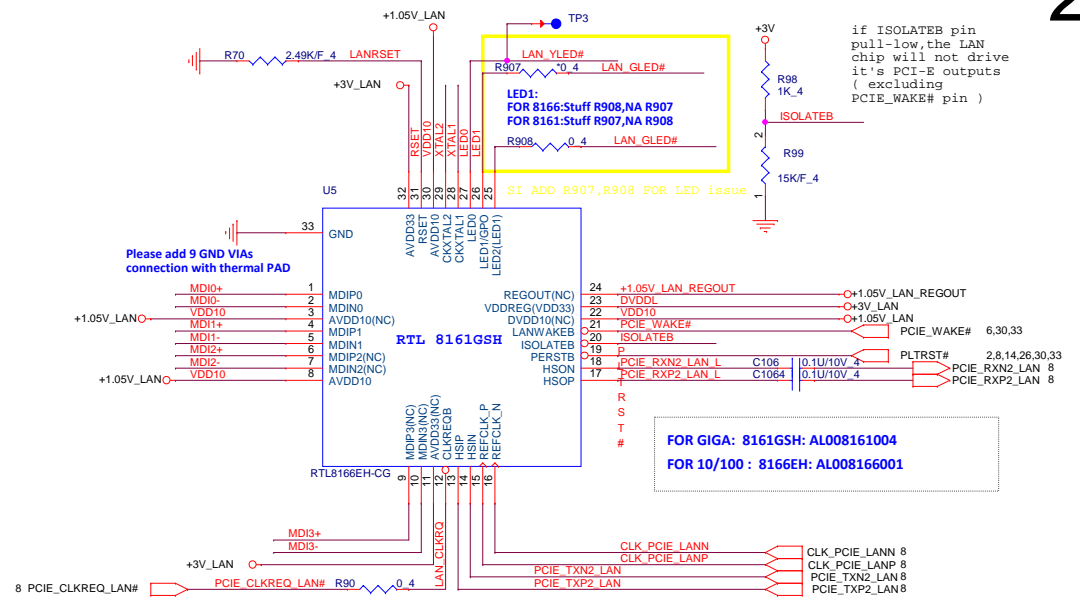
For 10/100
 * Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100
 * Stuff Ca and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
 * Stuff Ca and Cb only, close to each VDD3 pin-- 11, 32

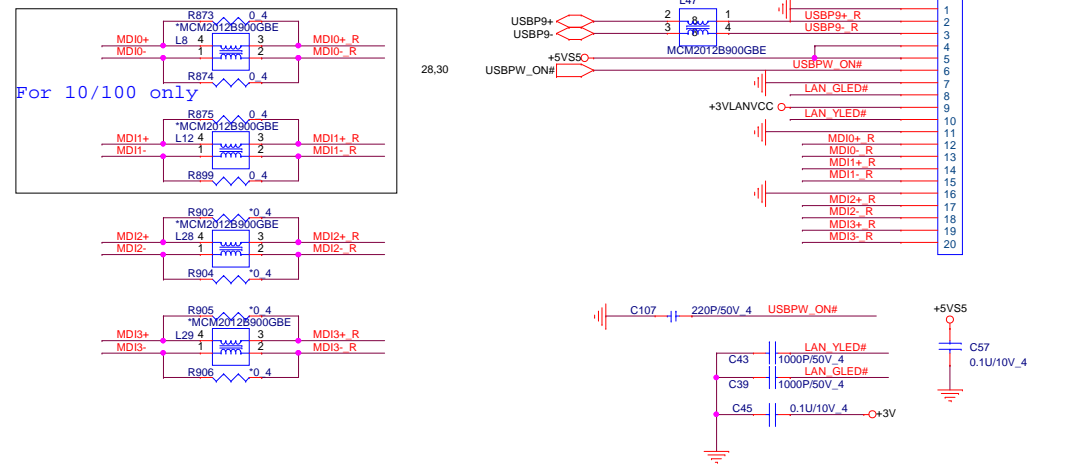


2,6,7,8,9,10,12,13,14,23,24,25,26,27,30,31,32,33,36,39,40,42, 25,39 +3VLANVCC

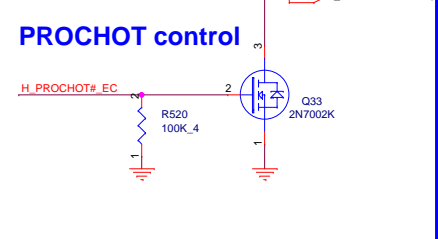
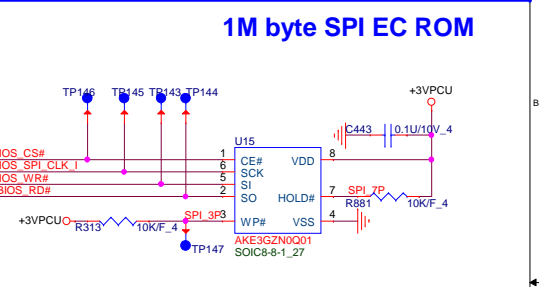
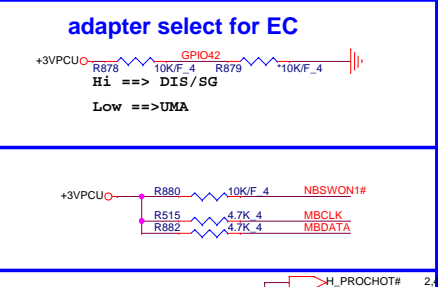
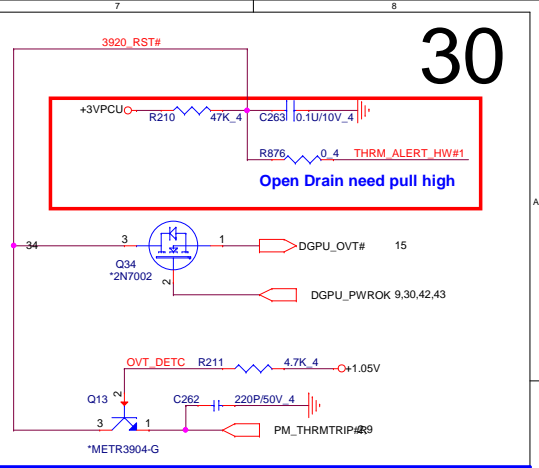
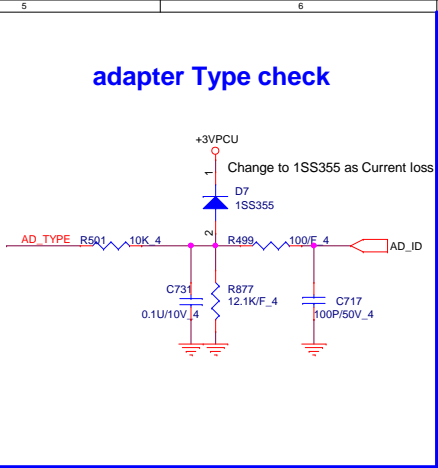
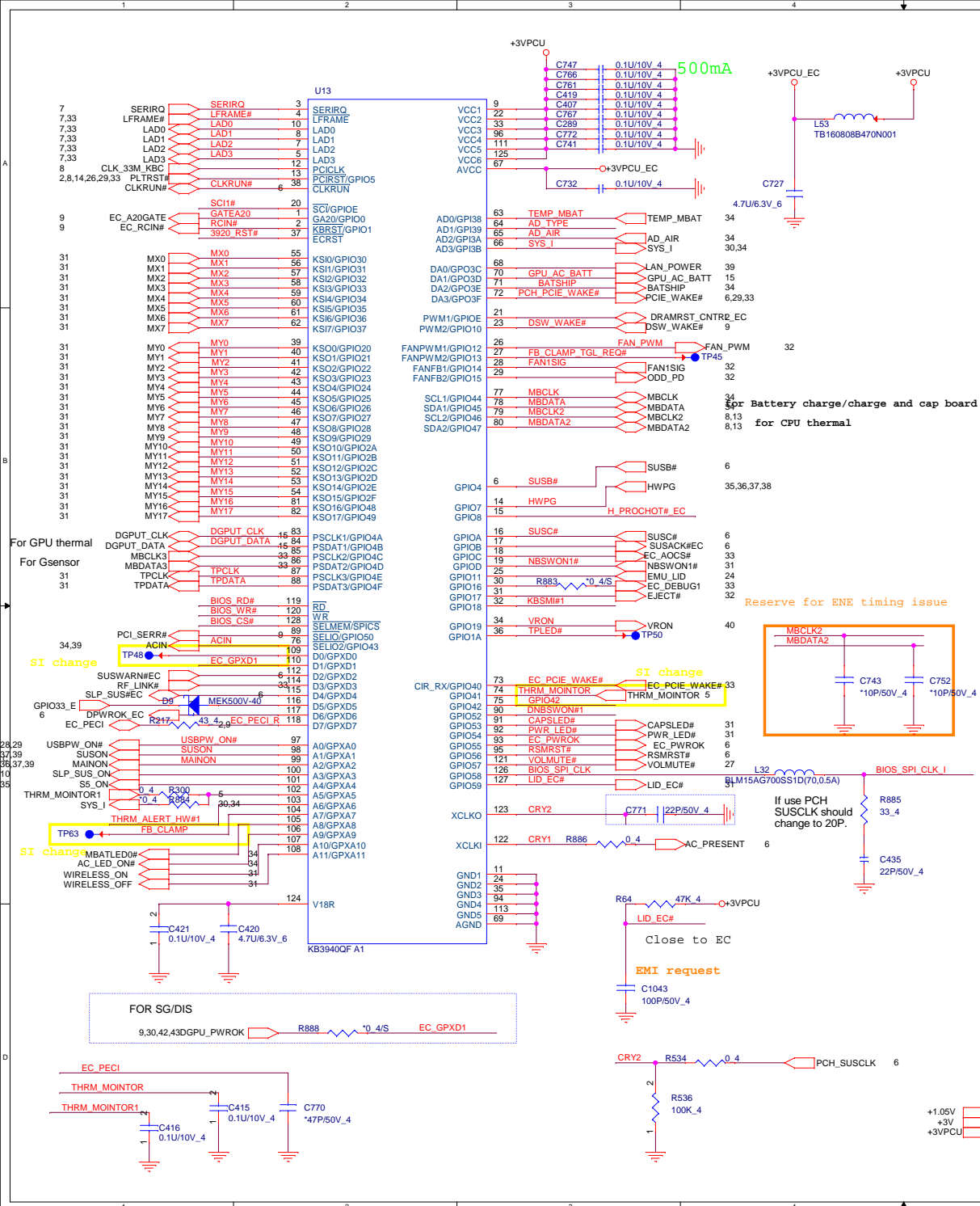


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

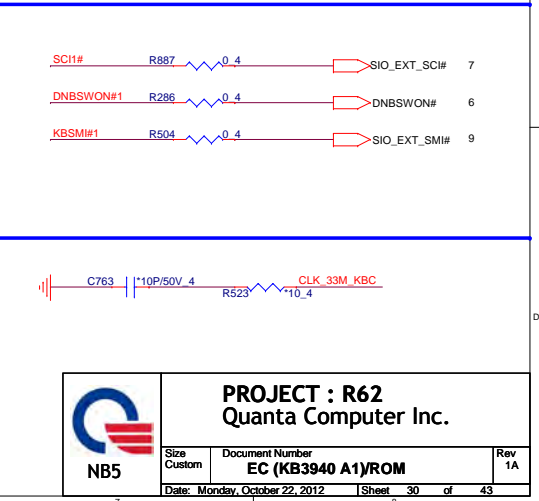
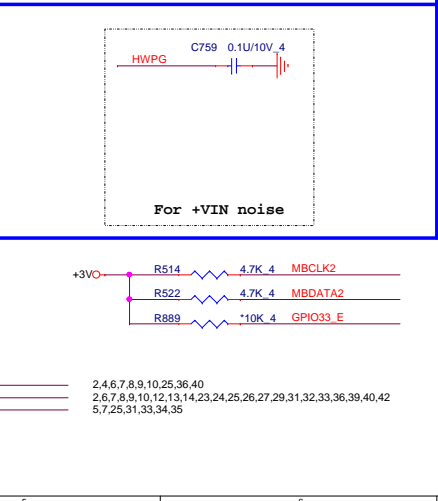
Right SIDE USBX1 and LAN CONN



	PROJECT : R62 Quanta Computer Inc.		
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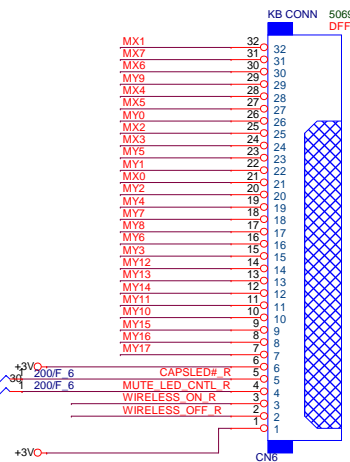
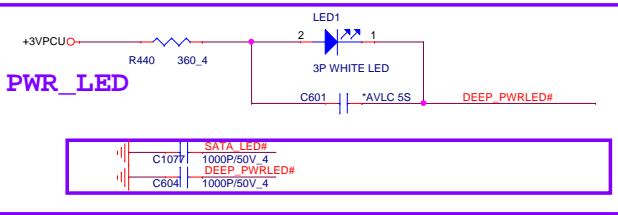
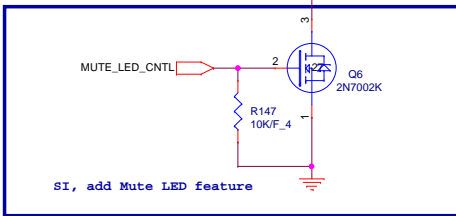
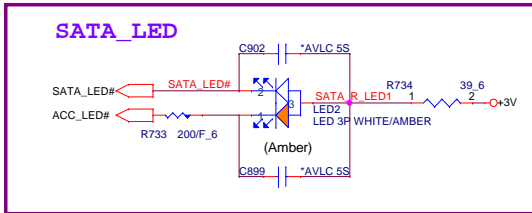
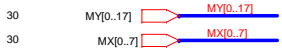
Vender	Size	P/N
EON	1MB	AKE3GN0Q01 (EN25Q80A-100HIP)
GigaDevice	1MB	AKE3GGN0Q00 (GD25Q80BSIGR)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023



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Quanta Computer Inc.

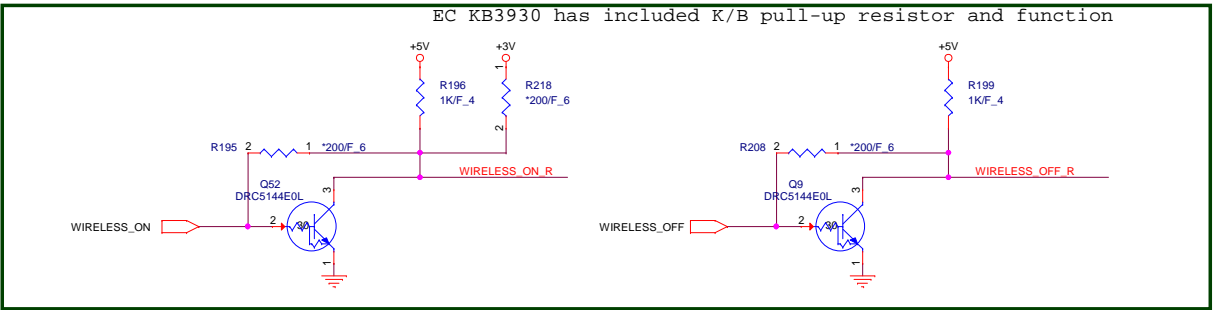
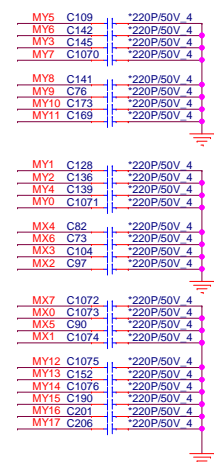
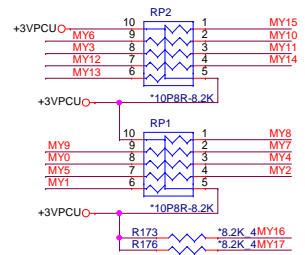
Size Custom	Document Number EC (KB3940 A1)ROM	Rev 1A
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KEYBOARD Con.



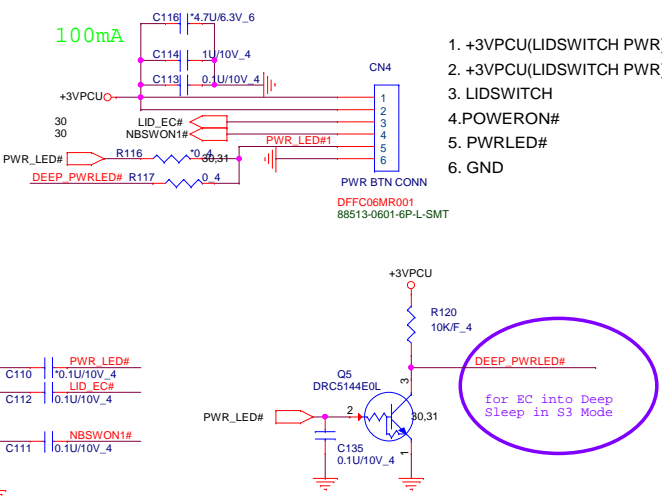
P/N update

KEYBOARD PULL-UP



EC KB3930 has included K/B pull-up resistor and function

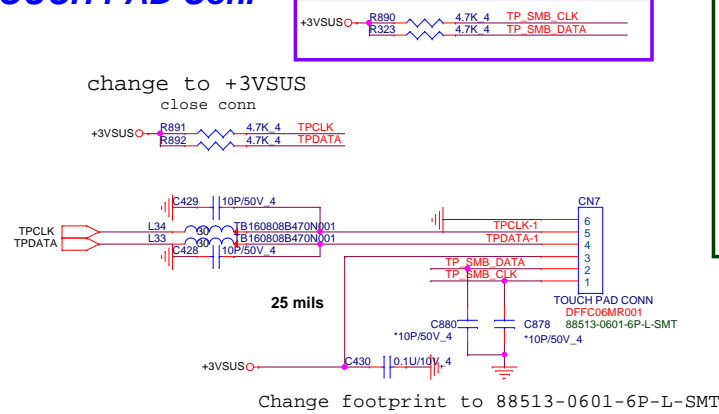
POWER BOTTON CONNECT



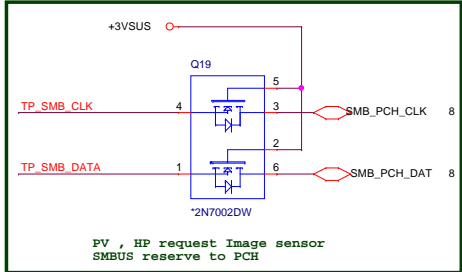
1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

for EC into Deep Sleep in S3 Mode

TOUCH PAD Con.



Change footprint to 88513-0601-6P-L-SMT



PV , HP request Image sensor SMBUS reserve to PCH

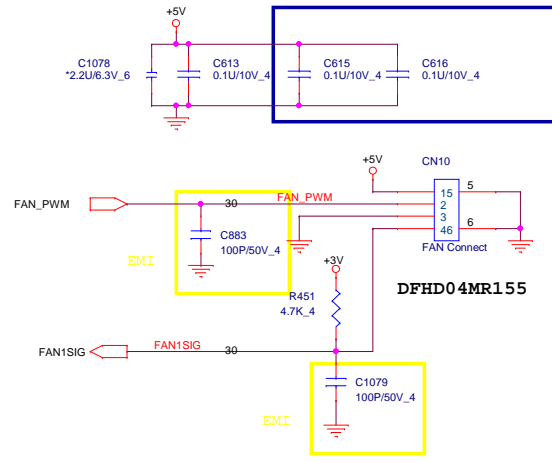


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Quanta Computer Inc.

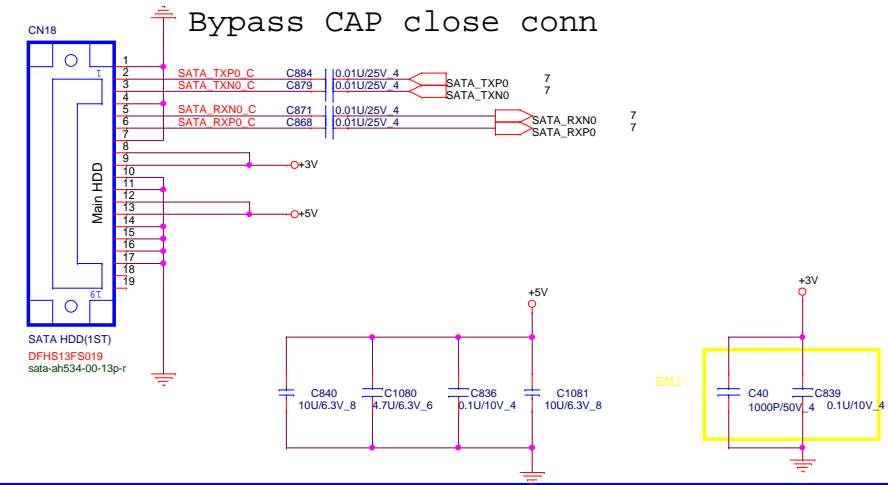
Size Custom	Document Number	Rev 1A
	LED/KB/SW/TP	

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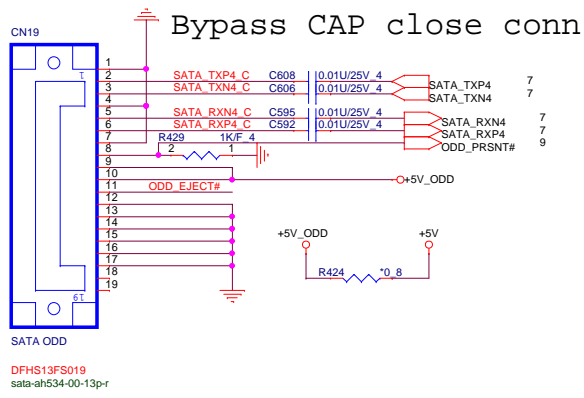
CPU FAN



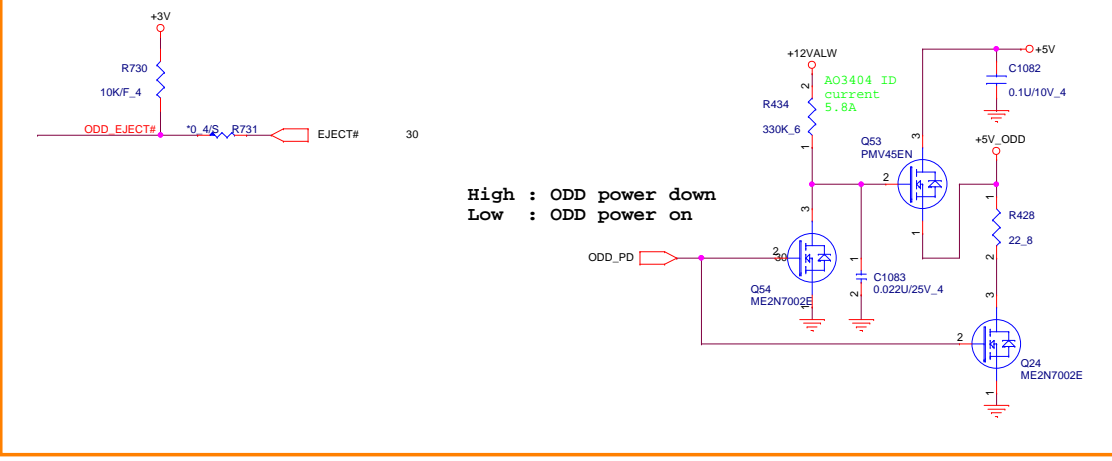
SATA HDD CONNECTOR



SATA ODD CONNECTOR



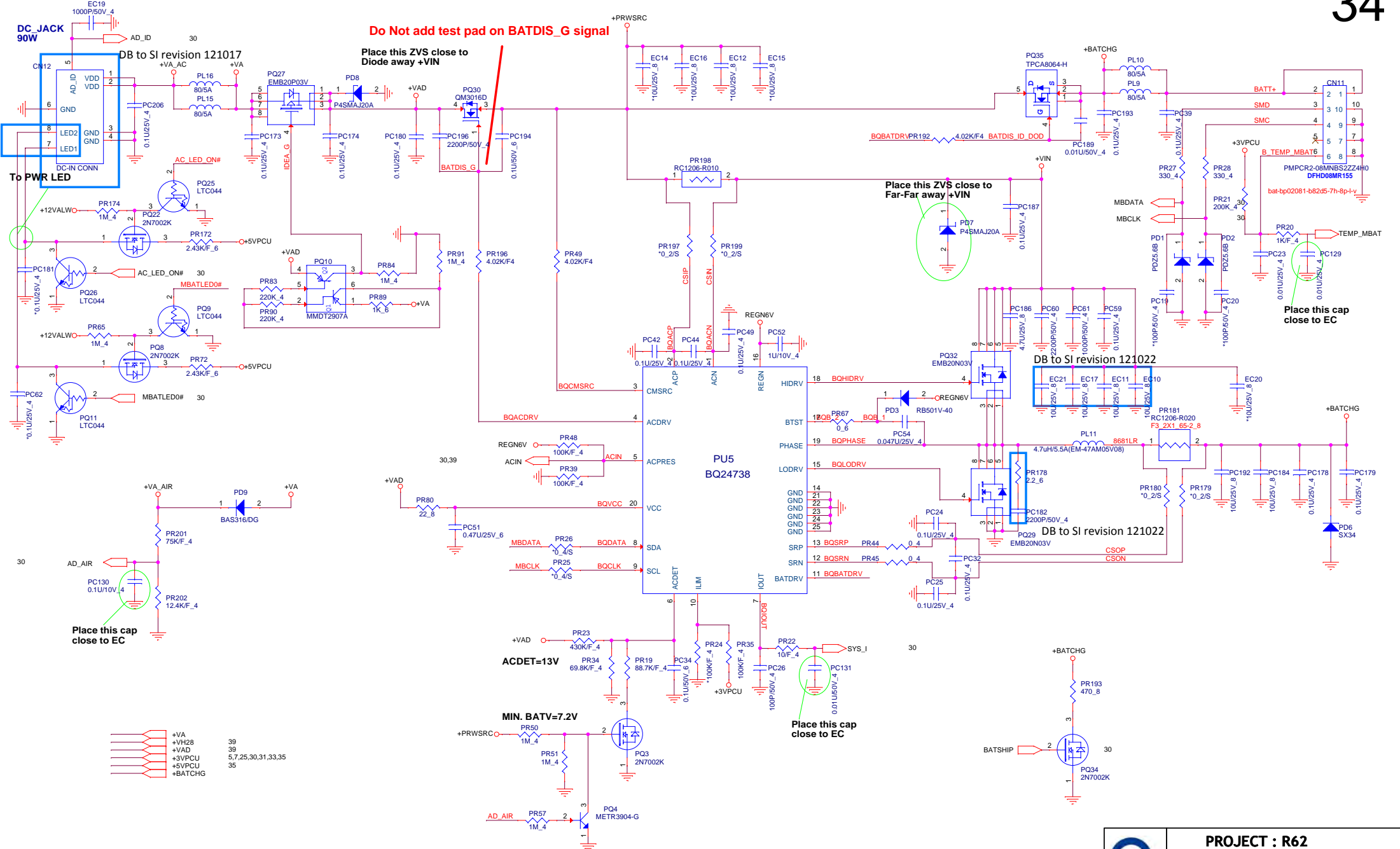
follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on

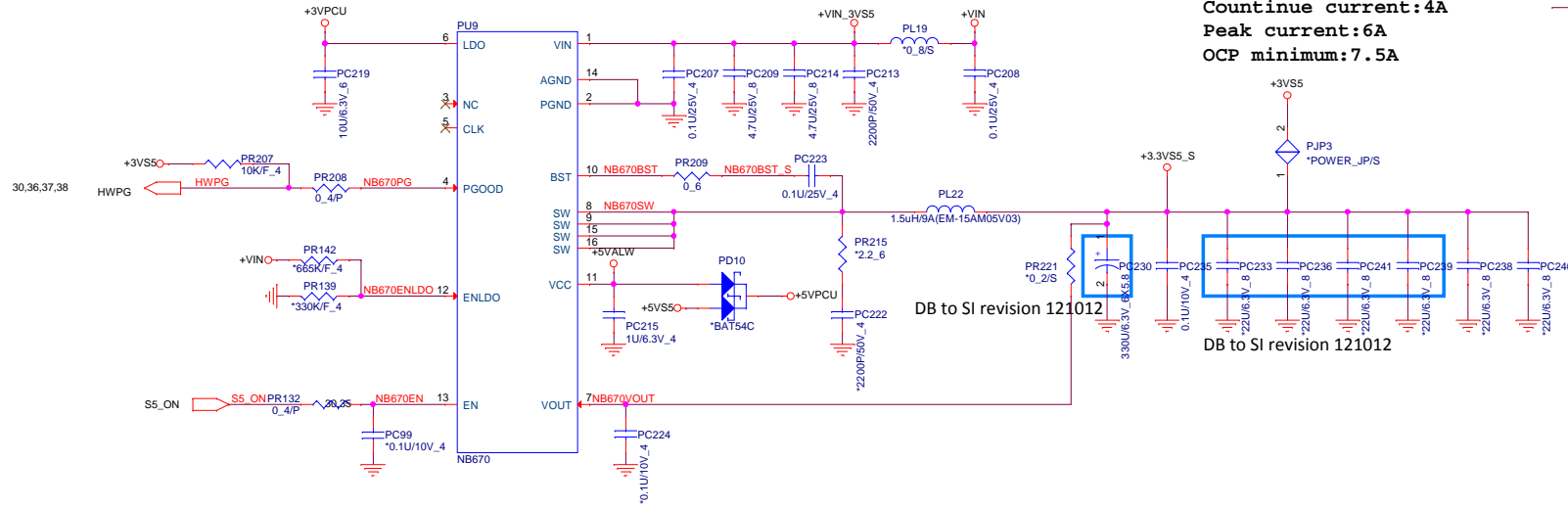
- +3V 2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,33,36,39,40,42
- +3VPCU 5,7,25,30,31,33,34,35
- +5V 7,10,23,25,27,31,33,39
- +12VALW 34,39,43

	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number HDD/ODD/FAN	Rev 1A
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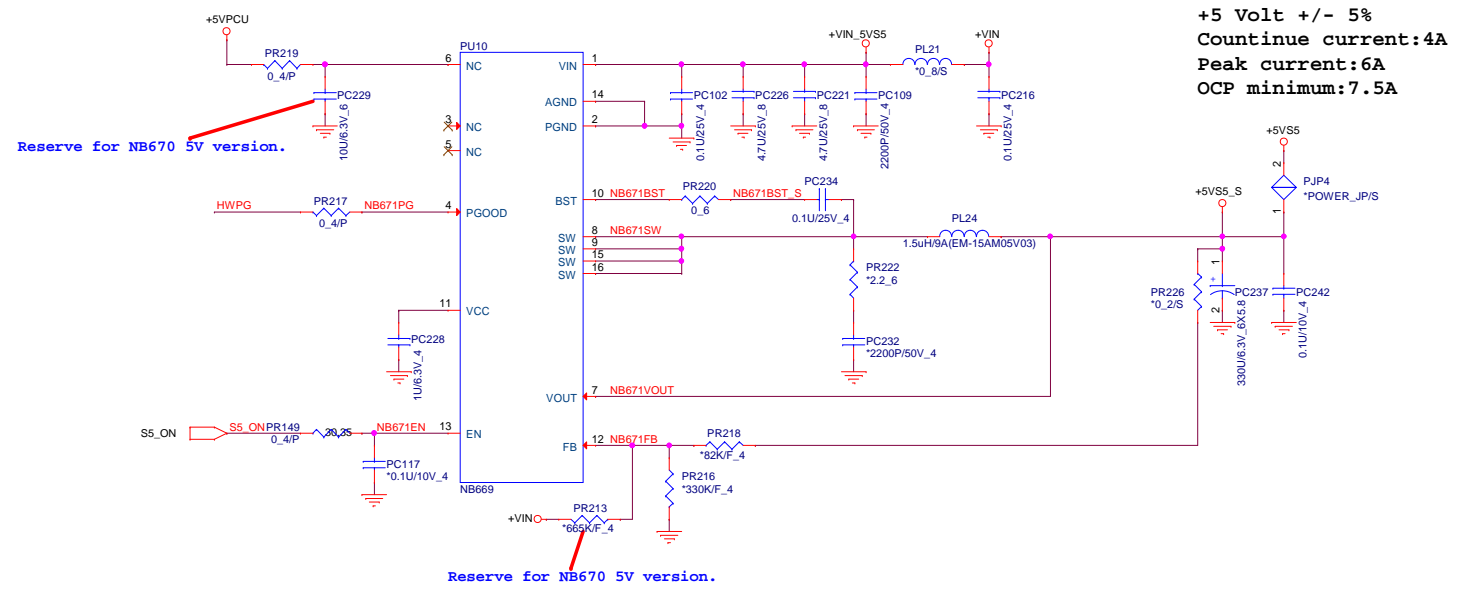


+VA	39
+VH28	39
+VAD	39
+3VPCU	5,7,25,30,31,33,35
+5VPCU	35
+BATCHG	35

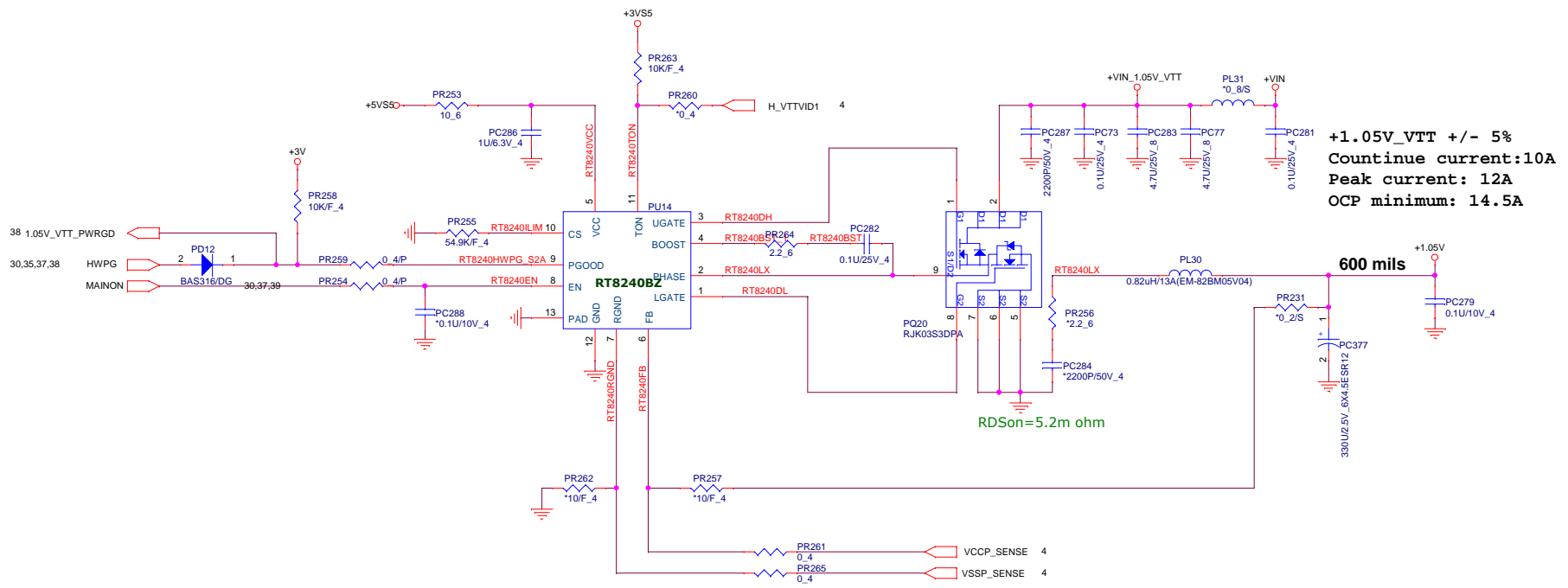
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom Document Number Charger (OZ8681)		
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+3VS5
 +5VS5
 6,7,9,10,33,36,39,43
 10,28,29,33,36,37,38,39,40,41,42,43



	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(RT8243A)	Rev 1A
	Date: Monday, October 22, 2012	Sheet 35 of 43	



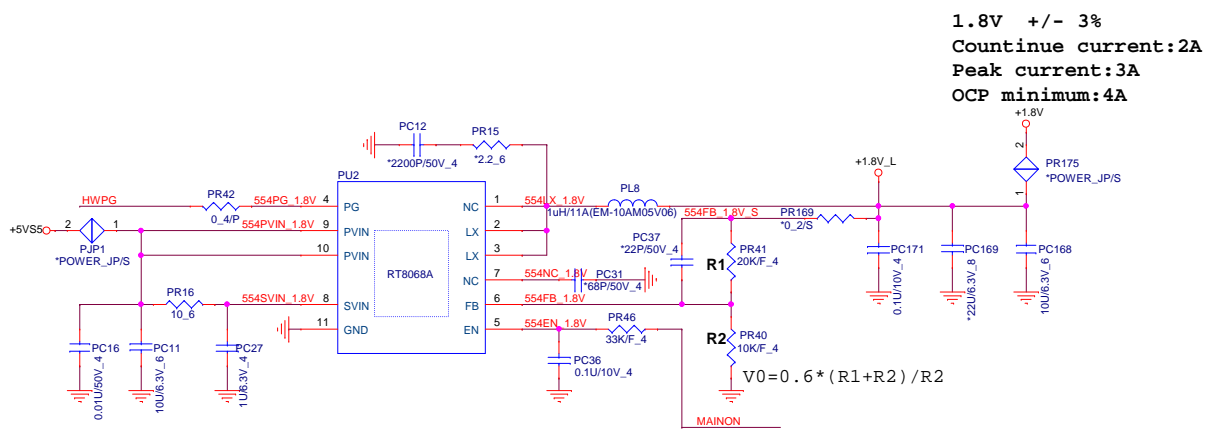
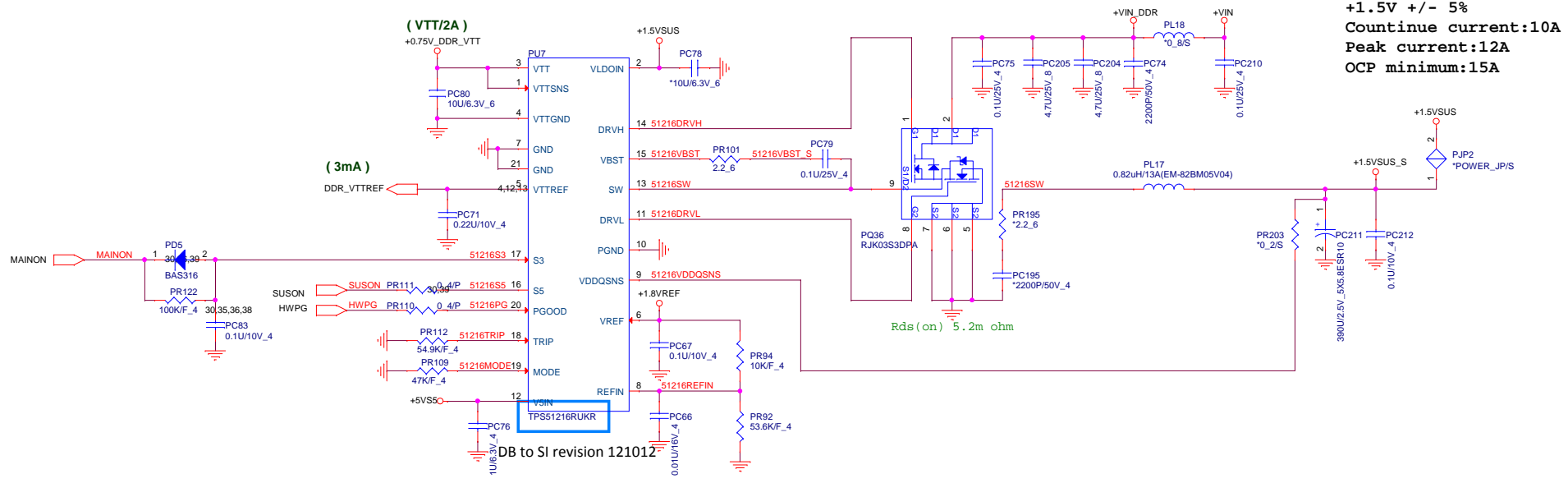
+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

600 mils

RDSon=5.2m ohm

+1.05V 2,4,6,7,8,9,10,25,30,40

	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number 1.05V(RT8228BZ)	
Date: Monday, October 22, 2012		Sheet 36 of 43	

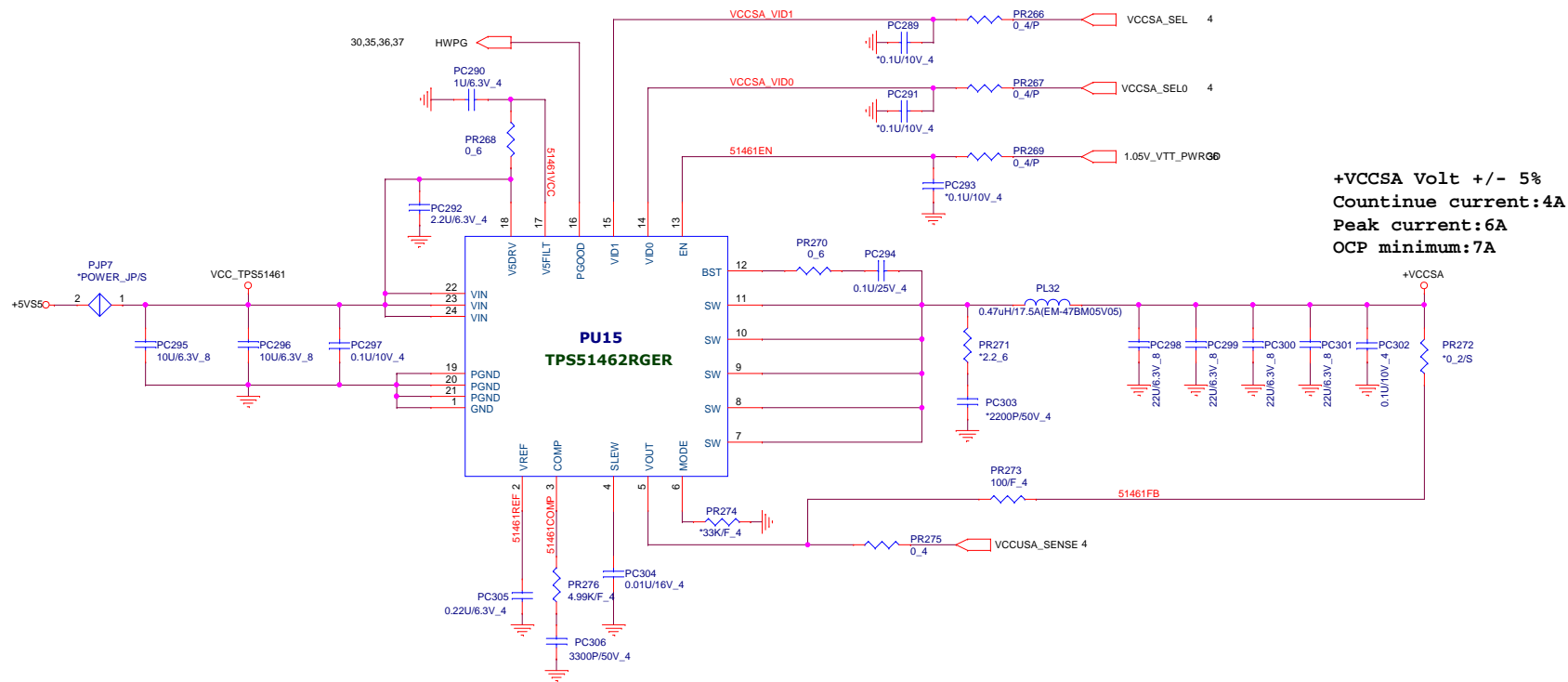


	PROJECT : R62		
	Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	DDR3L(APW8819)	1A
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TPSS1462RGER/AL051462000

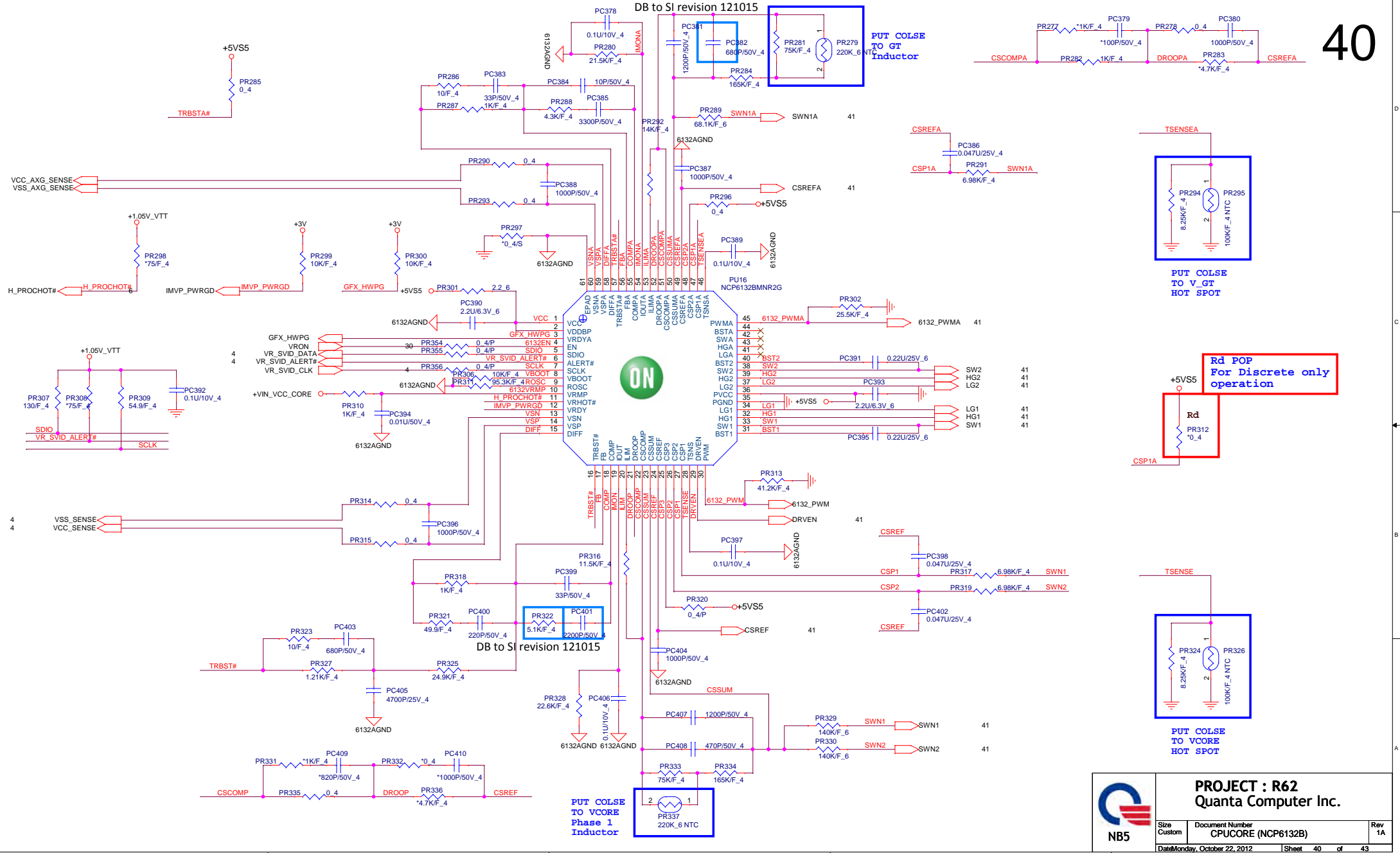
For CPU SV system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

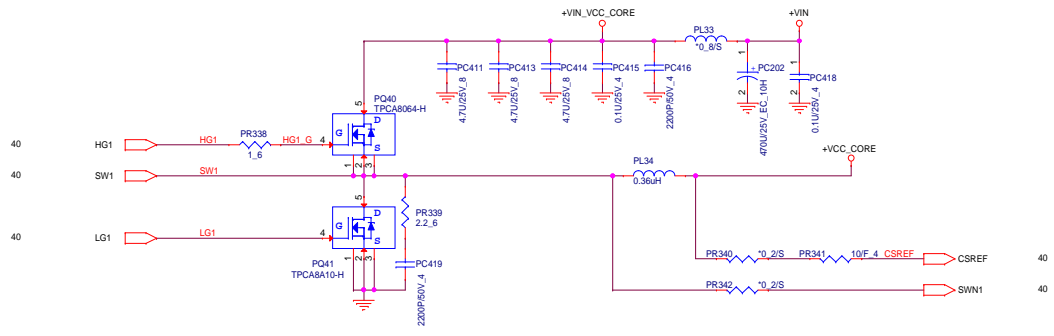


+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

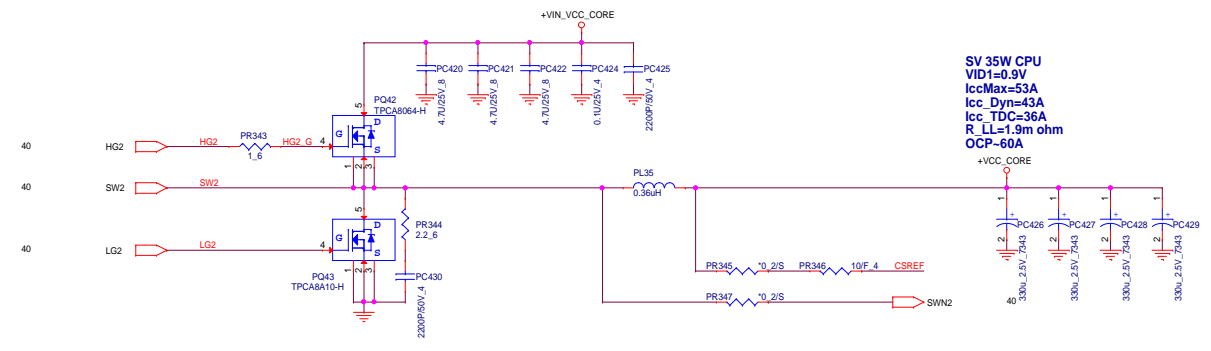
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number DDR3L(APW8819)	
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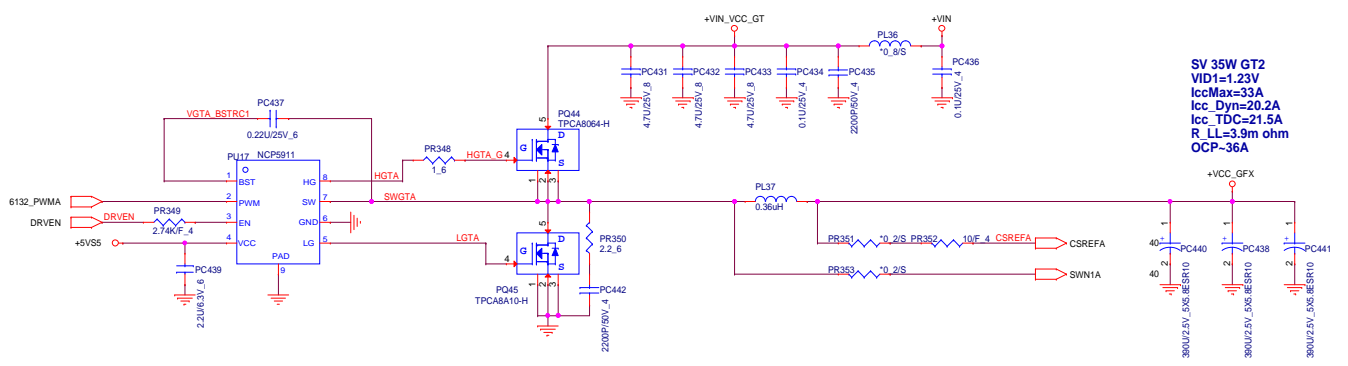
	PROJECT : R62	
	Quanta Computer Inc.	
	Size Custom	Document Number CPUCORE (NCP6132B)
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SV 35W CPU
 VID1=0.9V
 IccMax=53A
 Icc_Dyn=43A
 Icc_TDC=36A
 R_LL=1.9m ohm
 OCP-60A



SV 35W GT2
 VID1=1.23V
 IccMax=33A
 Icc_Dyn=20.2A
 Icc_TDC=21.5A
 R_LL=3.9m ohm
 OCP-36A



VGA Core

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

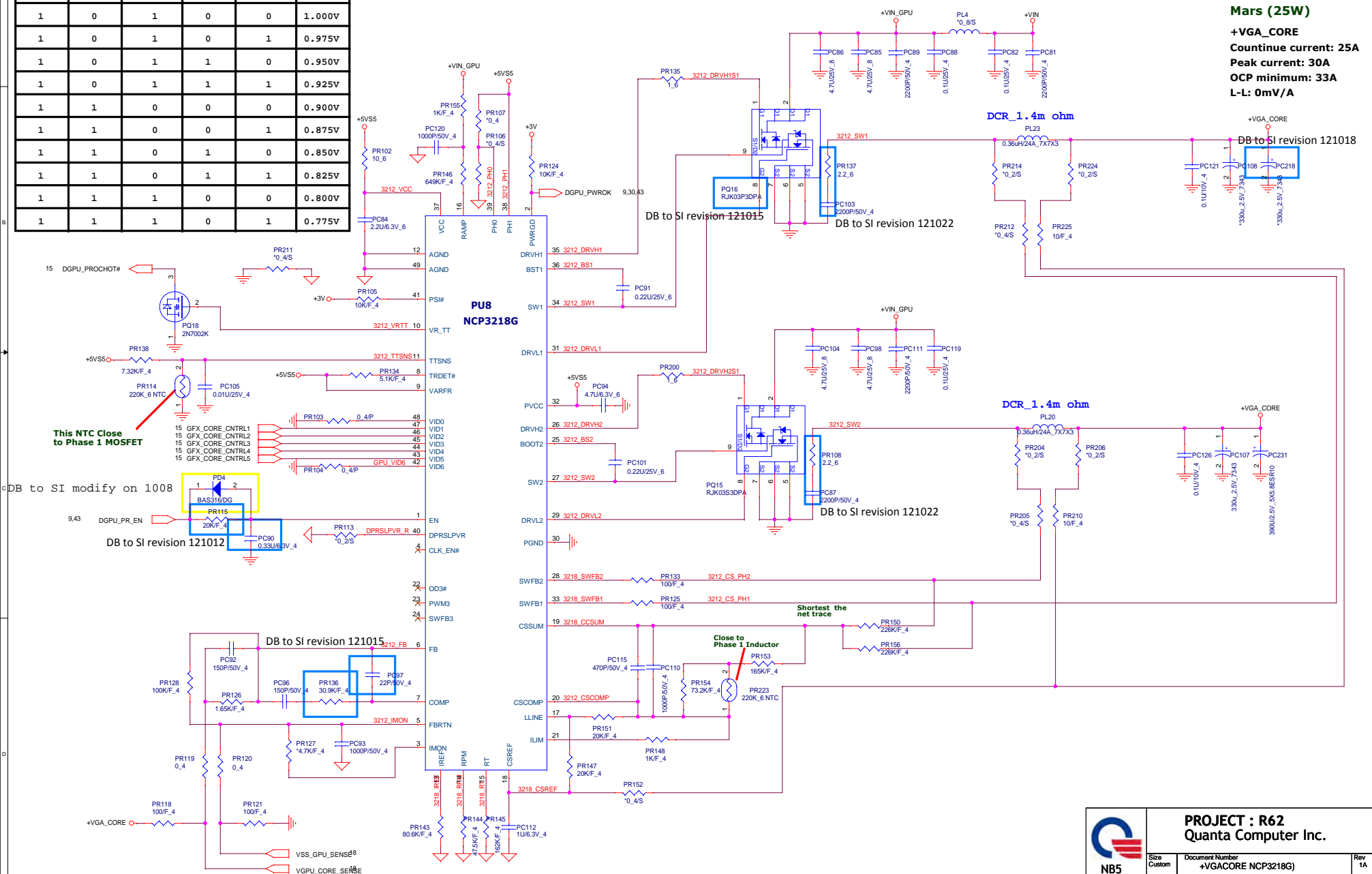
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

+VGA_CORE 18,33,43

Mars (25W)

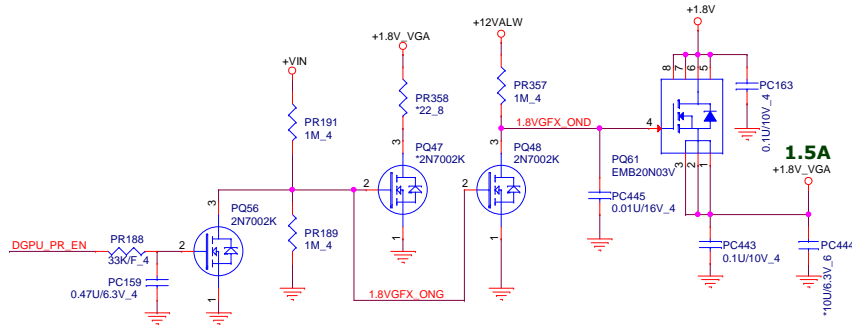
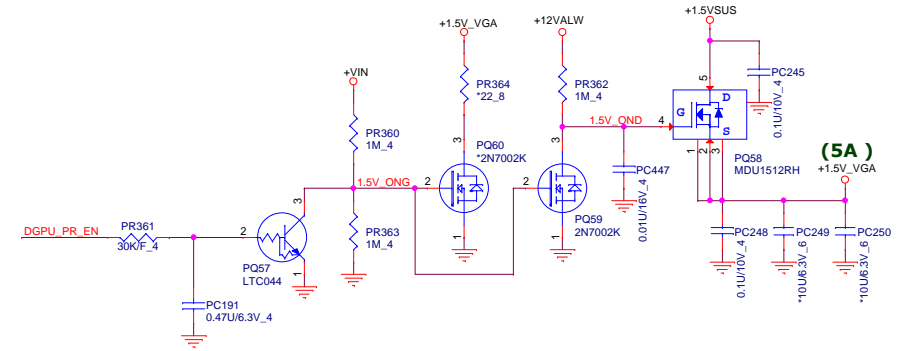
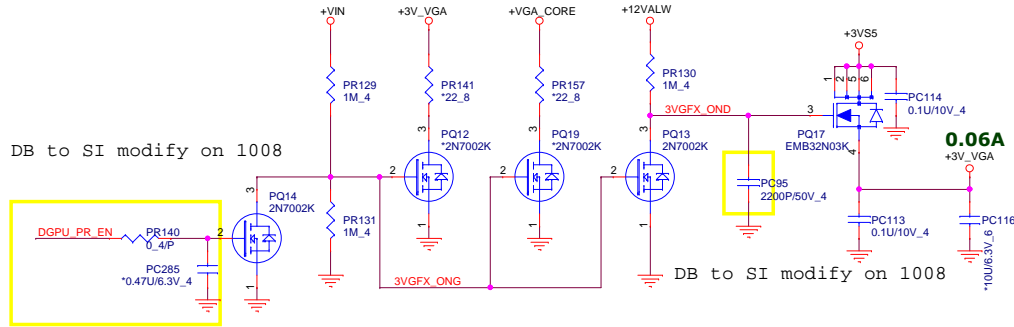
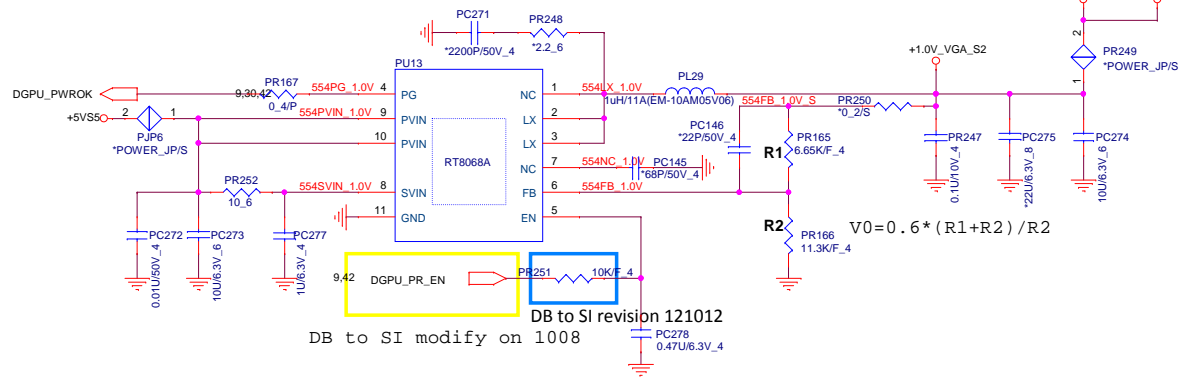
+VGA_CORE
 Continuum current: 25A
 Peak current: 30A
 OCP minimum: 33A
 L-L: 0mV/A



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R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



- +1.8V_VGA 15,16,18,19,25
- +1.0V_VGA 14,16,18,19
- +3V_VGA 18

	PROJECT : R62 Quanta Computer Inc.	
	Size Custom Document Number +VGACORE (RT8208/1.8V) Date: Monday, October 22, 2012	Rev 1A Sheet 43 of 43